

# Bolt Schematic

## Whiskey Lake

2018/12/12

REV : A00

*DY : None Installed*

*UMA: UMA only installed*

*OPS: DISCRTE OPTIMUS installed*

*TypeC: CCG4*

*TypeC\_5V\_OUT: provide external device power 5V*

*TypeC\_PWR\_IN: Provide system power via typeC connector.*

*8111H:Reltek LAN RTL811H*

*81106E:Reltek LAN RTL8106E*

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**BOLT WHL**

Rev

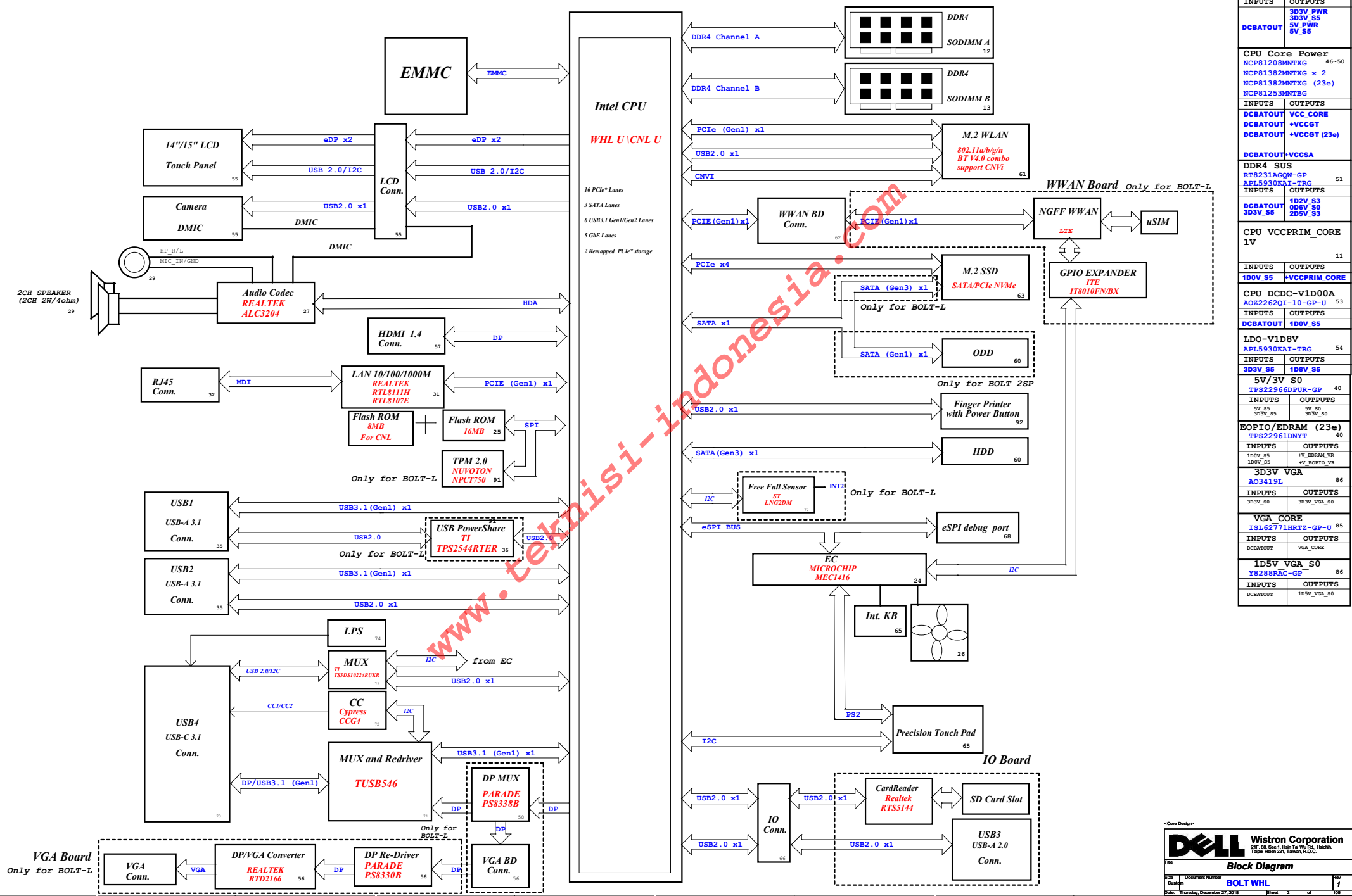
**1**

Date: Thursday, December 27, 2018

Sheet 1 of 105

Project Code : QRQY00000009  
PCB P/N : 17938  
Revision : 1

# Bolt WHL Block Diagram

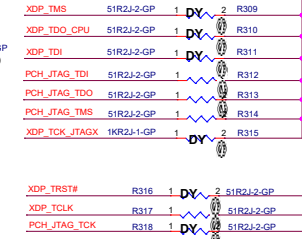
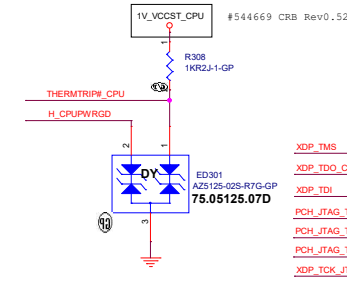
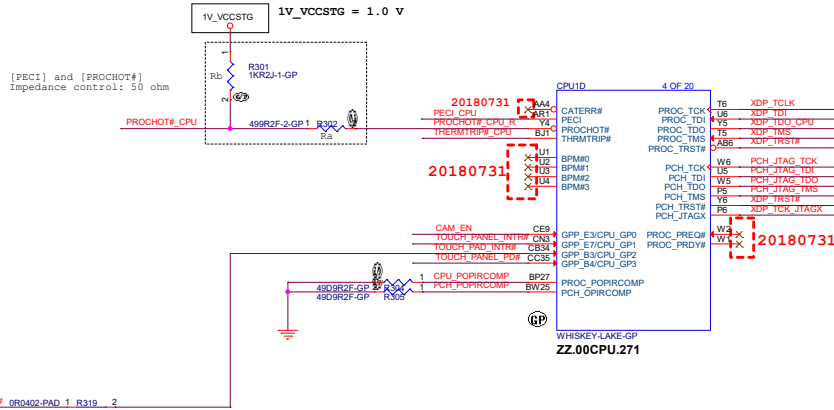


CHARGER	
ISL95522/ISL9538	44
INPUTS	
AD+	DCBATOUT
SYSTEM DC/DC	
TP51225RUKR-GP	45
INPUTS	
DCBATOUT	303V PWR 303V S5 5V PWR 5V S5
CPU Core Power	
NCBP81208MNTXG	46-50
NCBP81382MNTXG x 2	
NCBP81382MNTXG (23e)	
NCBP81253MNTBG	
INPUTS	
DCBATOUT	VCC CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT+VCCSA	
DDR4 SUS	
RT8231AGW-GP	51
APL5930KAI-TRG	
INPUTS	
DCBATOUT	102V S3 303V S5
CPU VCCPRIM_CORE	
1V	11
INPUTS	
100V S5	+VCCPRIM CORE
CPU DCDC-V1D00A	
A022262QI-10-GP-U	53
INPUTS	
DCBATOUT	100V S5
LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	
303V S5	108V S5
5V/3V S0	
TPS22966DPUR-GP	40
INPUTS	
5V S5 303V S5	5V S0 303V S0
EOP10/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	
100V S5 100V S5	+V EDRAM VR +V EOP10 VR
3D3V VGA	
A03419L	86
INPUTS	
303V S0	303V VGA_S0
VGA CORE	
ISL6271HRTZ-GP-U	85
INPUTS	
DCBATOUT	VGA_CORE
1D5V VGA S0	
Y8288RAC-GP	86
INPUTS	
DCBATOUT	1D5V VGA_S0

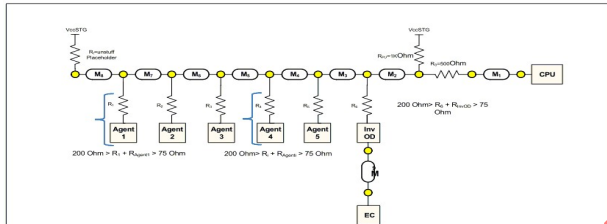
# Main FUNC = CPU

24 PECL\_CPU  
24.44.46 PROCHOT#\_CPU  
55 TOUCH\_PANEL\_INTR#  
24.65 TP\_WAKE\_KBC#  
55 TOUCH\_PANEL\_PDR#  
17 H\_CPUWIRGD

55 CAM\_EN



## (#575412) PROCHOT# Routing Guidelines



## Main FUNC = CPU

## HDMI 1.4B

57 HDMI\_DDI\_TX\_N0 <<<  
57 HDMI\_DDI\_TX\_P0 <<<  
57 HDMI\_DDI\_TX\_N1 <<<  
57 HDMI\_DDI\_TX\_P1 <<<  
57 HDMI\_DDI\_TX\_N2 <<<  
57 HDMI\_DDI\_TX\_P2 <<<  
57 HDMI\_DDI\_TX\_N3 <<<  
57 HDMI\_DDI\_TX\_P3 <<<  
57 CPU\_DP1\_CTRL\_CLK <<<  
57 CPU\_DP1\_CTRL\_DATA <<<  
57 CPU\_DP1\_HPD <<<

## TO DP MUX

58 DP2\_DDI\_TX\_N0 <<<  
58 DP2\_DDI\_TX\_P0 <<<  
58 DP2\_DDI\_TX\_N1 <<<  
58 DP2\_DDI\_TX\_P1 <<<  
58 DP2\_DDI\_TX\_N2 <<<  
58 DP2\_DDI\_TX\_P2 <<<  
58 DP2\_DDI\_TX\_N3 <<<  
58 DP2\_DDI\_TX\_P3 <<<  
58 DP2\_AUX\_CPU\_P <<<  
58 DP2\_AUX\_CPU\_N <<<  
58 DP2\_HPD\_CPU >>>

## EDP

55 eDP\_TX\_CPU\_N0 <<<  
55 eDP\_TX\_CPU\_P0 <<<  
55 eDP\_TX\_CPU\_N1 <<<  
55 eDP\_TX\_CPU\_P1 <<<  
55 eDP\_AUX\_CPU\_N <<<  
55 eDP\_AUX\_CPU\_P <<<  
55 EDP\_HPD >>>

24 L\_BKLT\_EN <<<  
55 L\_BKLT\_CTRL <<<  
55 EDP\_VDD\_EN <<<

61 CNVI\_ENW <<<

## 5.2.7 Compensation Signal Routing Guidelines

Signal	Trace	Termination	Resistor Value	Max Length
402_40202	1.0mm	50ohm	330 0.1% 0.5W	500mm

## 5.2.8 eDP Disabling and Termination Guidelines

Signal	Trace	Termination
402_40202	1.0mm	No connect
402_40202	1.0mm	No connect
402_40202	1.0mm	No connect
402_40202	1.0mm	No connect

## #543016 DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Table 9-1. Pin Straps (Sheet 3 of 4)

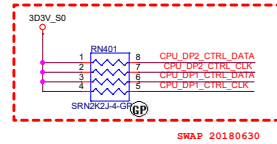
Signal	Usage	When Sampled	Comment
SPIO_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2SD_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. <b>Notes:</b> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPB_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. <b>Notes:</b> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPB_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. <b>Notes:</b> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz (PLL) is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RST_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVI enable. 1 = Integrated CNVI disable.

#566439

Signal	Usage	When Sampled	Comment
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% <b>Note:</b> This strap should only be used for specific targeted 1S battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. <b>Warning:</b> This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

Pin Straps (Sheet 4 of 4)

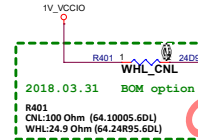
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SWAP 20180630

## HDMI 1.4B

## TO DP MUX



2018.03.31 BOM option

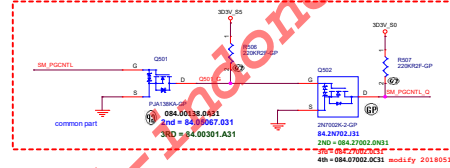
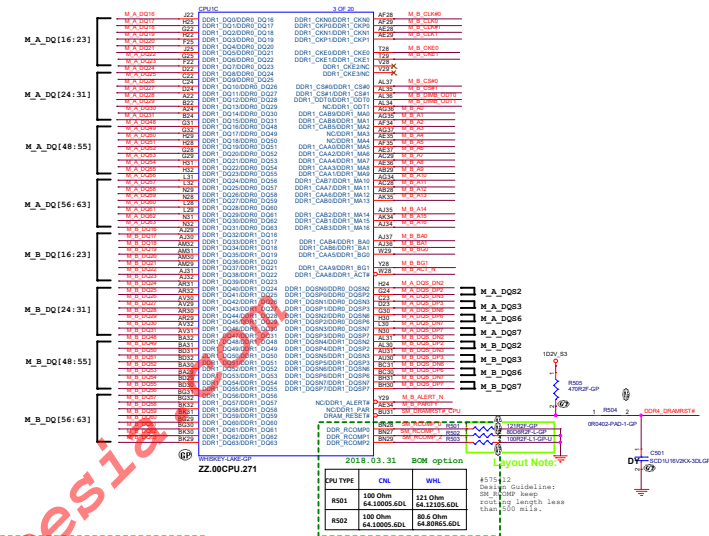
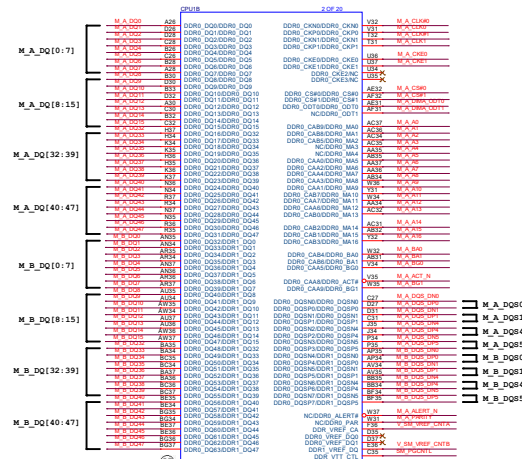
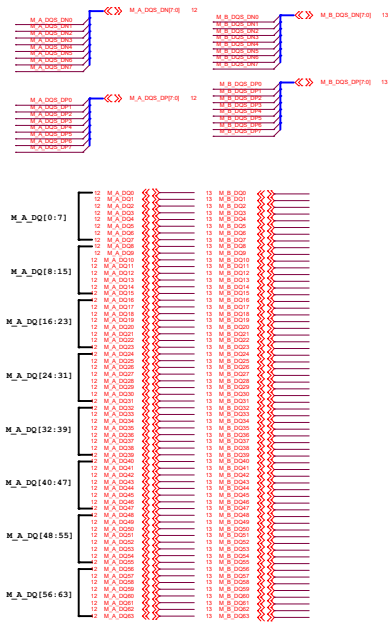
CNL100 Ohm (64.10005.6DU)

WHL24.9 Ohm (64.24955.6DU)

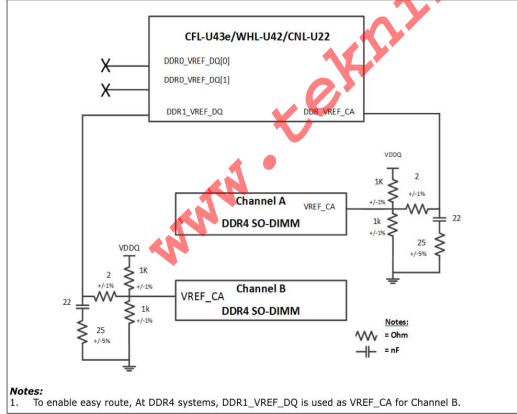
HDMI\_DDI\_TX\_N0 ALS  
HDMI\_DDI\_TX\_P0 ALS  
HDMI\_DDI\_TX\_N1 ALS  
HDMI\_DDI\_TX\_P1 ALS  
HDMI\_DDI\_TX\_N2 AFS  
HDMI\_DDI\_TX\_P2 AFS  
HDMI\_DDI\_TX\_N3 AFS  
HDMI\_DDI\_TX\_P3 AFS  
CPU\_DP1\_CTRL\_CLK  
CPU\_DP1\_CTRL\_DATA  
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CPU\_DP198\_HPD\_P  
CPU\_DP199\_CTRL\_CLK  
CPU\_DP199\_CTRL\_DATA  
CPU\_DP199\_HPD  
CPU\_DP199\_HPD\_N  
CPU\_DP199\_HPD\_P  
CPU\_DP200\_CTRL\_CLK



DDR4 ball type: Non-Interleaved Type



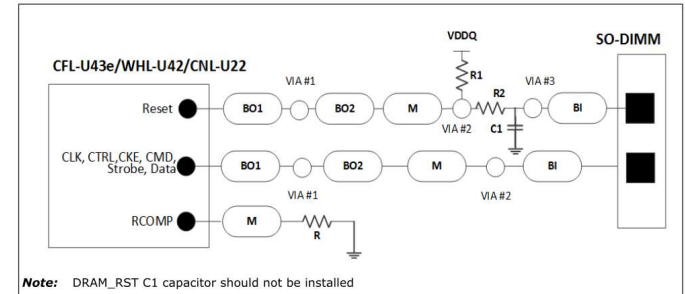
**Figure 4-1. WHL U DDR4 SODIMM V<sub>REF-CA</sub> Overview**



**Notes:**

1. To enable easy route, At DDR4 systems, DDR1\_VREF\_DQ is used as VREF\_CA for Channel B.

## WHL U DDR4 SODIMM T3/8L Signals Topologies



**Note:** DRAM\_RST C1 capacitor should not be installed

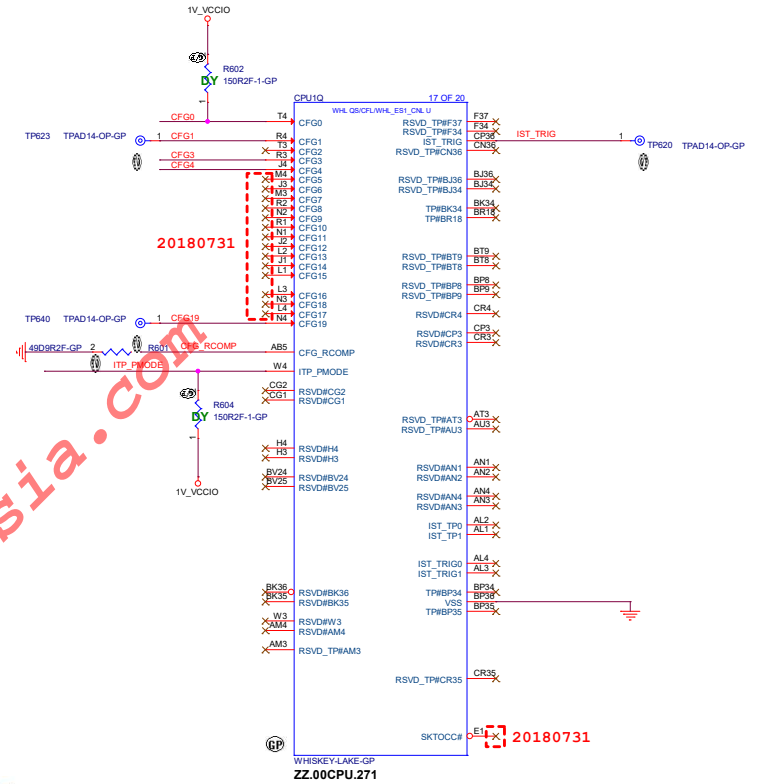
RCOMP (0/1/2)	M	US/SL	500			15	20	25	CFL-U43e/ WHL-U42; 121/80.6/ 100  CNL-U22; 100/100/ 100
Reset	BO1	US	500	8000		3		6	R1=470 [5%] R2=0 C1=0.1uF (no stuff)
	BO2	SL	800-BO1			3.5		12	
	M	SL			50	4		20	
	BI	US				4		20	

BOLT L 14 ENAC



File		<b>CPU (DDR)</b>		
Size	Document Number			
Custom	<b>BOLT WHL</b>			
Date:	Thursday, December 27, 2018	Sheet	5	of 10

**Main FUNC = CPU**



**Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1**

	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIE_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS  DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS  DDR_RCOMP[2]: 162Ω ± 1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS  DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS  DDR_RCOMP[2]: 100Ω ± 1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

```

46 VDDCORE_SENSE <<< <<< <<<
46 VSSCORE_SENSE <<< <<< <<<

46 SVD_DATA_CPU <<< <<< <<<
46 SVD_CLK_CPU <<< <<< <<<
46 SVD_ALERT#_CPU <<< <<< <<<

```

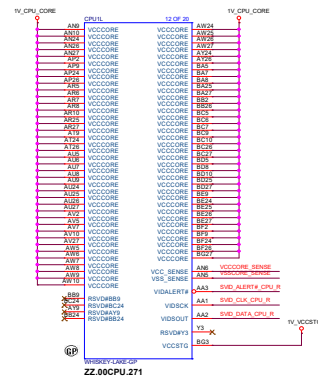


Figure 10: Schematic diagram of the 1000BASE-SX optical module. The diagram shows three optical modules connected to a central 'CLOSE TO CPU' block. The top module is labeled 'TV\_MDC01\_CPU' and contains a 'R7005 1000SFP-1.0P-U' component. The middle module is labeled 'TV\_MDC01\_CPU' and contains a 'R7005 5402PFC-1.0P-U' component. The bottom module is labeled 'TV\_MDC01\_CPU' and contains a 'R7004 1000SFP-1.0P-U' component. Each module is connected to a 'SMD\_DATA\_CPU' or 'SMD\_ALS01A\_CPU' line. The connections are labeled with '1' and '2' and 'R7001' or 'R7002'.

[illegible]

<p>It represents 4 signals: VIDSOUT#, VIDSK, VIDSALERT# and VIDSRES#.</p>	
SVID Signals	VIDSOUT, VIDSK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSK platform resistors	Rpu1=Empty, Rpu2=450, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=560, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

#575412

IMV/P8/B Controller

Vss\_SENSE

Vcc\_SENSE

R1

Vcc Plane

Vss Plane

R2

R1-R2 100 ohm catch resistors

Die

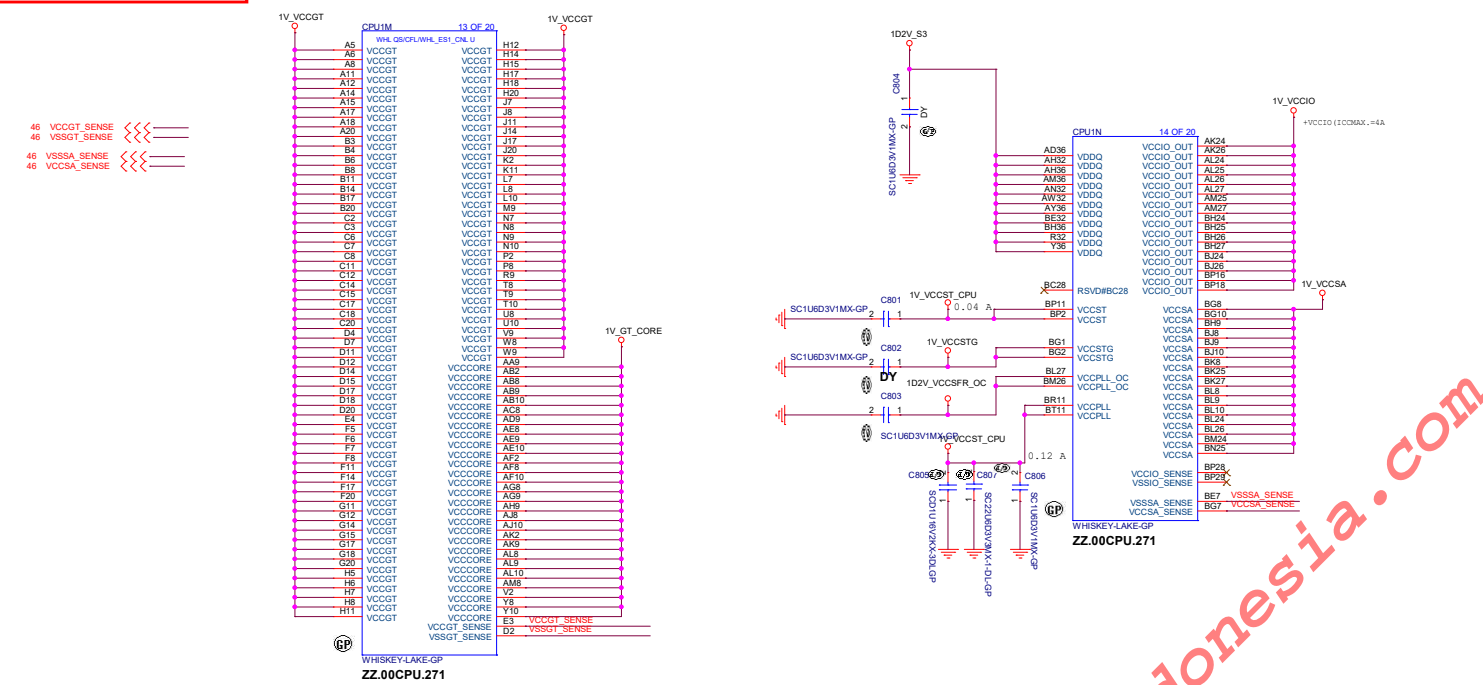
Processor Package

Socket

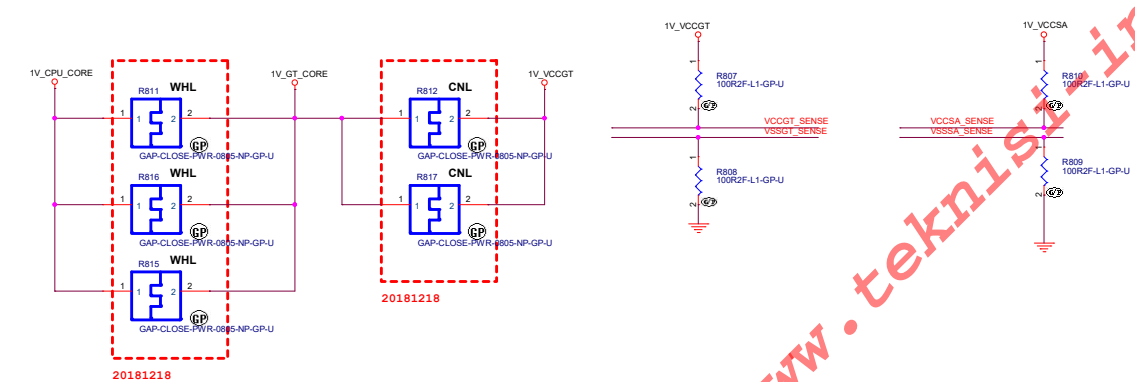
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
Vcc <sub>GT</sub> _SENSE / Vss <sub>GT</sub> _SENSE			
Vcc <sub>SA</sub> _SENSE / Vss <sub>SA</sub> _SENSE			
Vcc <sub>IO</sub> _SENSE / Vss <sub>IO</sub> _SENSE <sup>(1)</sup>			
		NA	

- R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to V<sub>CC</sub>\_SENSE/V<sub>SS</sub>\_SENSE line resistance.

Main FUNC = CPU



Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



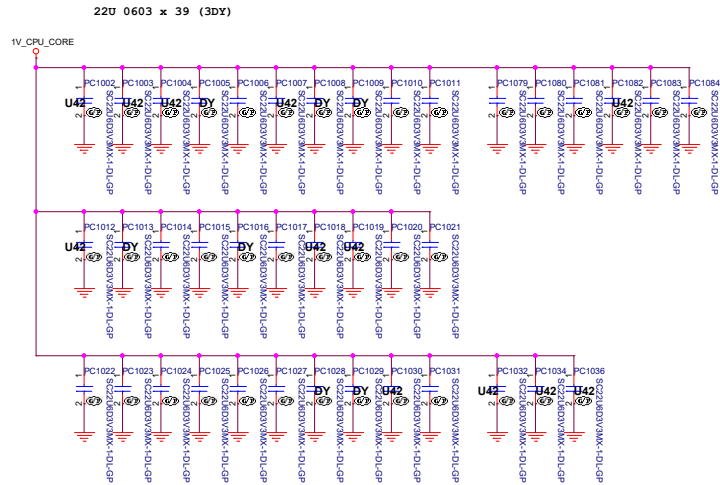
Design Target	CPU support	Stuffing options for compatibility	Incremental VR BOM vs KBL	Incremental board area vs. KBL
Cost optimized entry design (C13-SMB0-ICP)	CNL only	None	No increase expected for CNL vs. KBL U22	~0mm² vs. KBL U22
Premium design (C17-C13)	WHL only	None	Load line change anticipated to drive incremental cost vs. KBL R	TBD
Scalable mainstream design (C17-ICP)	WHL and CNL	Jumpers vary by SKU: 3 if WHL 1 if CNL	Load line change on WHL anticipated to drive incremental cost vs. KBL R No increase expected for CNL vs. KBL U22	TBD

Main Func = CPU

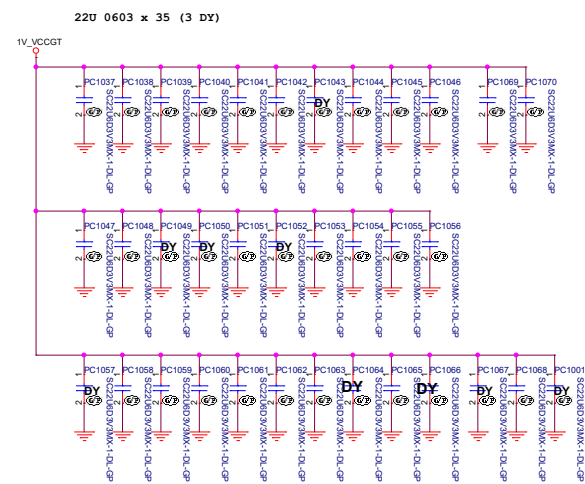
(Blanking)

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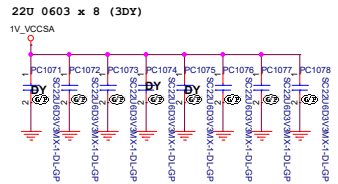
1V\_CPU\_CORE



VCCGT



VCCSA



KBL-R U42 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR) 1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
VDDQ Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCPLL Power Plane at V1P0A VR output	1x 0.1uF 0402	Placed at primary side near to VR output

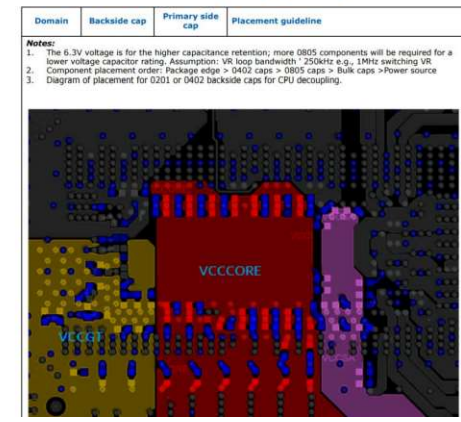
**Notes:**

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

KBL-R U42 Decoupling Requirements (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
VCCGT	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
VCCSA	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
VCCIO		4x 1 uF 0402	Place as close to the package as possible
VDDQ		4x 10 uF 0402	Place as close to the package as possible
VDDQ		3 x 22 uF 0603	Place as close to the package as possible
VDDQ		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQ BGA routing should not exceed 48mm (RdC). RVP design uses trace L=450um, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
VCCPLL		1x 1 uF 0402	Place as close to the package as possible.
VCCPLL_OC		1x 1 uF 0201	Do not route VCCPLL, VCCPLL_OC, VCCGT closest adjacent layer over any power net other than ground.
VCCGT		1x 1 uF 0402	For VCCST: Refer to Figure 48-2 for additional routing details for VCCST & VCCSTG.

KBL-R U42 Decoupling Requirements (Sheet 2 of 2)

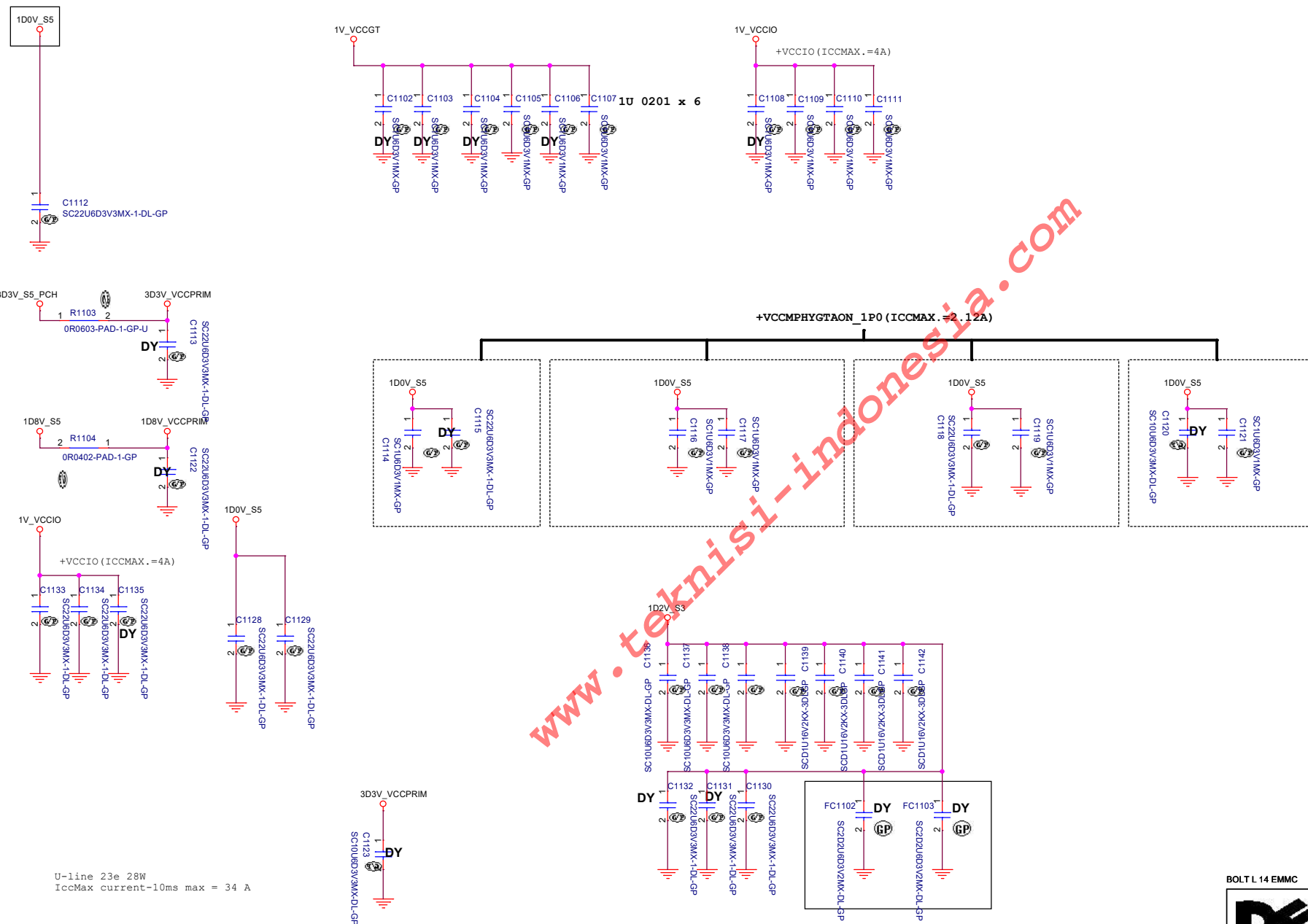


BOLT L14 EMMC



Main FUNC = CPU

# PCH DERIVED RAILS UNSLICED GT VCCIO



U-line 23e 28W  
IccMax current-10ms max = 34 A

RF request 2016/01/12 modify

**Layout Note:**  
1uF:  
C1174 near N15  
C1180 near K15  
C1173 near AF20  
C1172 near N18  
C1175 near AB19  
22uF :  
C1182 C1184 near N15  
10uF:  
C1176 near N15

BOLT L 14 EMMC

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>CPU_(Power CAP2)</b>			
Size A3	Document Number	Rev <b>1</b>	
Date: Thursday, December 27, 2018		Sheet 11	of 105



Main Func  
= MEMORY

M\_A\_DQS\_DN0 M\_A\_DQS\_DN1 M\_A\_DQS\_DN2 M\_A\_DQS\_DN3 M\_A\_DQS\_DN4 M\_A\_DQS\_DN5 M\_A\_DQS\_DN6 M\_A\_DQS\_DN7 M\_A\_DQS\_DP0 M\_A\_DQS\_DP1 M\_A\_DQS\_DP2 M\_A\_DQS\_DP3 M\_A\_DQS\_DP4 M\_A\_DQS\_DP5 M\_A\_DQS\_DP6 M\_A\_DQS\_DP7

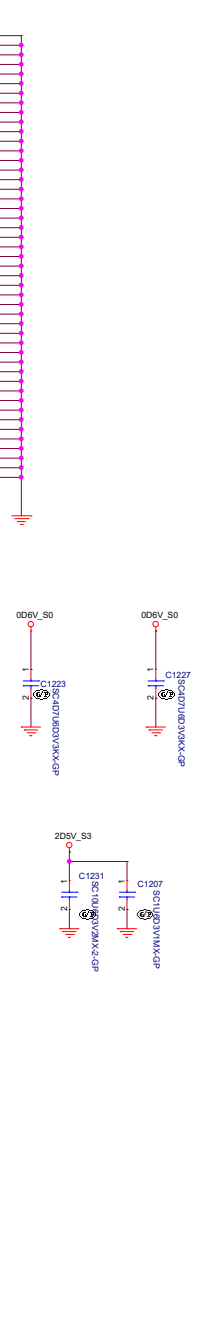
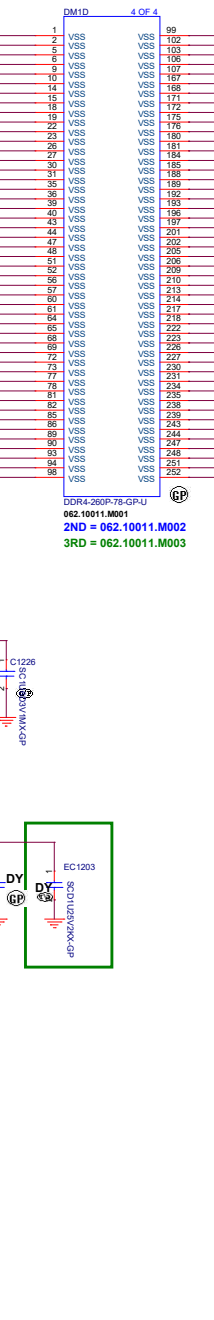
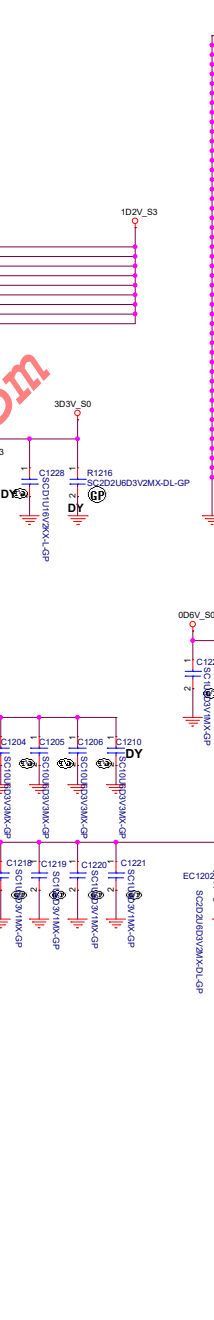
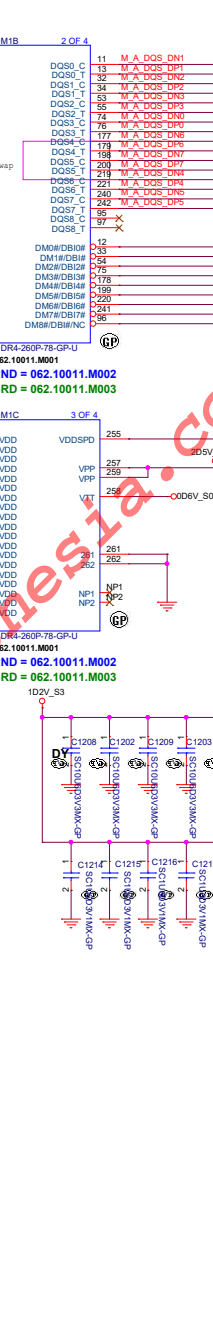
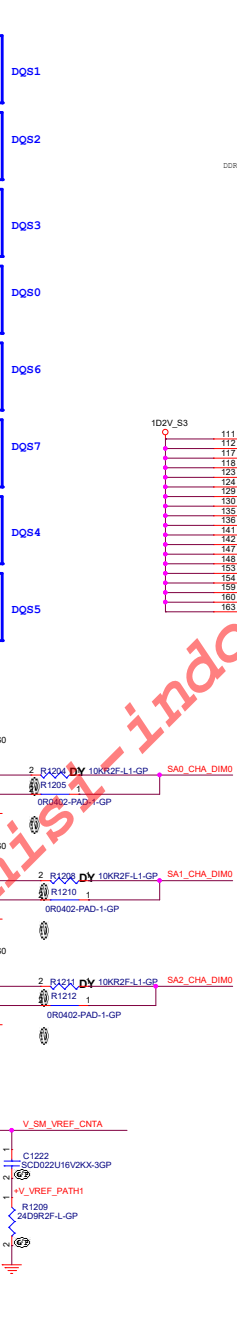
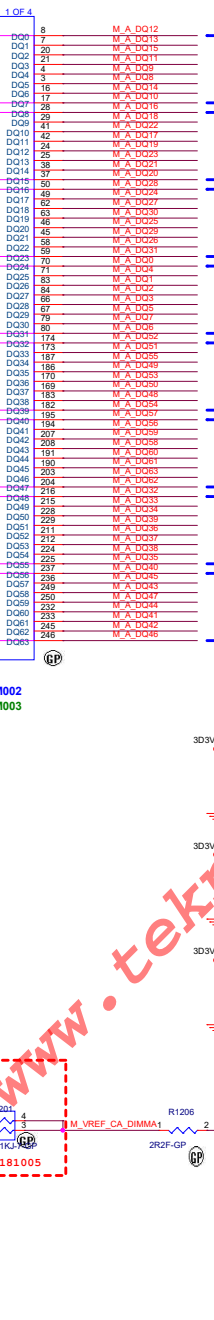
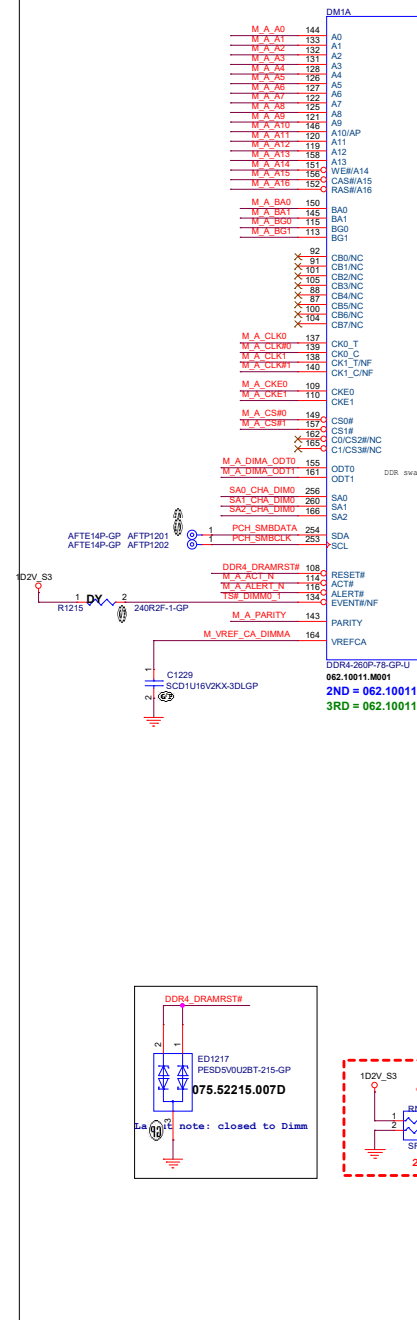
M\_A\_A0 5 M\_A\_A1 5 M\_A\_A2 5 M\_A\_A3 5 M\_A\_A4 5 M\_A\_A5 5 M\_A\_A6 5 M\_A\_A7 5 M\_A\_A8 5 M\_A\_A9 5 M\_A\_A10 5 M\_A\_A11 5 M\_A\_A12 5 M\_A\_A13 5 M\_A\_A14 5 M\_A\_A15 5 M\_A\_A16 5

M\_A\_DQ0 5 M\_A\_DQ1 5 M\_A\_DQ2 5 M\_A\_DQ3 5 M\_A\_DQ4 5 M\_A\_DQ5 5 M\_A\_DQ6 5 M\_A\_DQ7 5 M\_A\_DQ8 5 M\_A\_DQ9 5 M\_A\_DQ10 5 M\_A\_DQ11 5 M\_A\_DQ12 5 M\_A\_DQ13 5 M\_A\_DQ14 5 M\_A\_DQ15 5 M\_A\_DQ16 5 M\_A\_DQ17 5 M\_A\_DQ18 5 M\_A\_DQ19 5 M\_A\_DQ20 5 M\_A\_DQ21 5 M\_A\_DQ22 5 M\_A\_DQ23 5 M\_A\_DQ24 5 M\_A\_DQ25 5 M\_A\_DQ26 5 M\_A\_DQ27 5 M\_A\_DQ28 5 M\_A\_DQ29 5 M\_A\_DQ30 5 M\_A\_DQ31 5 M\_A\_DQ32 5 M\_A\_DQ33 5 M\_A\_DQ34 5 M\_A\_DQ35 5 M\_A\_DQ36 5 M\_A\_DQ37 5 M\_A\_DQ38 5 M\_A\_DQ39 5 M\_A\_DQ40 5 M\_A\_DQ41 5 M\_A\_DQ42 5 M\_A\_DQ43 5 M\_A\_DQ44 5 M\_A\_DQ45 5 M\_A\_DQ46 5 M\_A\_DQ47 5 M\_A\_DQ48 5 M\_A\_DQ49 5 M\_A\_DQ50 5 M\_A\_DQ51 5 M\_A\_DQ52 5 M\_A\_DQ53 5 M\_A\_DQ54 5 M\_A\_DQ55 5 M\_A\_DQ56 5 M\_A\_DQ57 5 M\_A\_DQ58 5 M\_A\_DQ59 5 M\_A\_DQ60 5 M\_A\_DQ61 5 M\_A\_DQ62 5 M\_A\_DQ63 5

M\_A\_DIMA\_ODT0 5 M\_A\_DIMA\_ODT1 5

PCH\_SMBDATA 13,18,56,70 PCH\_SMBCLK 13,18,56,70

DDR4\_DRAMRST# 5,13 M\_A\_ACT\_N 5 M\_A\_ALERT\_N 5 M\_A\_PARITY 5 M\_A\_BA0 5 M\_A\_BA1 5 M\_A\_BG0 5 M\_A\_BG1 5 V\_SM\_VREF\_CNTA 5



```

M_B_A0 5
M_B_A1 5
M_B_A2 5
M_B_A3 5
M_B_A4 5
M_B_A5 5
M_B_A6 5
M_B_A7 5
M_B_A8 5
M_B_A9 5
M_B_A10 5
M_B_A11 5
M_B_A12 5
M_B_A13 5
M_B_A14 5
M_B_A15 5
M_B_A16 5

M_B_BA0 5
M_B_BA1 5
M_B_BG0 5
M_B_BG1 5

M_B_CLK0 5
M_B_CLK9 5
M_B_CLK1 5
M_B_CLKF1 5

M_B_CKD0 5
M_B_CKE1 5

M_B_CS0 5
M_B_CS1 5

M_B_DIMB_COT
M_B_DIMB_COT

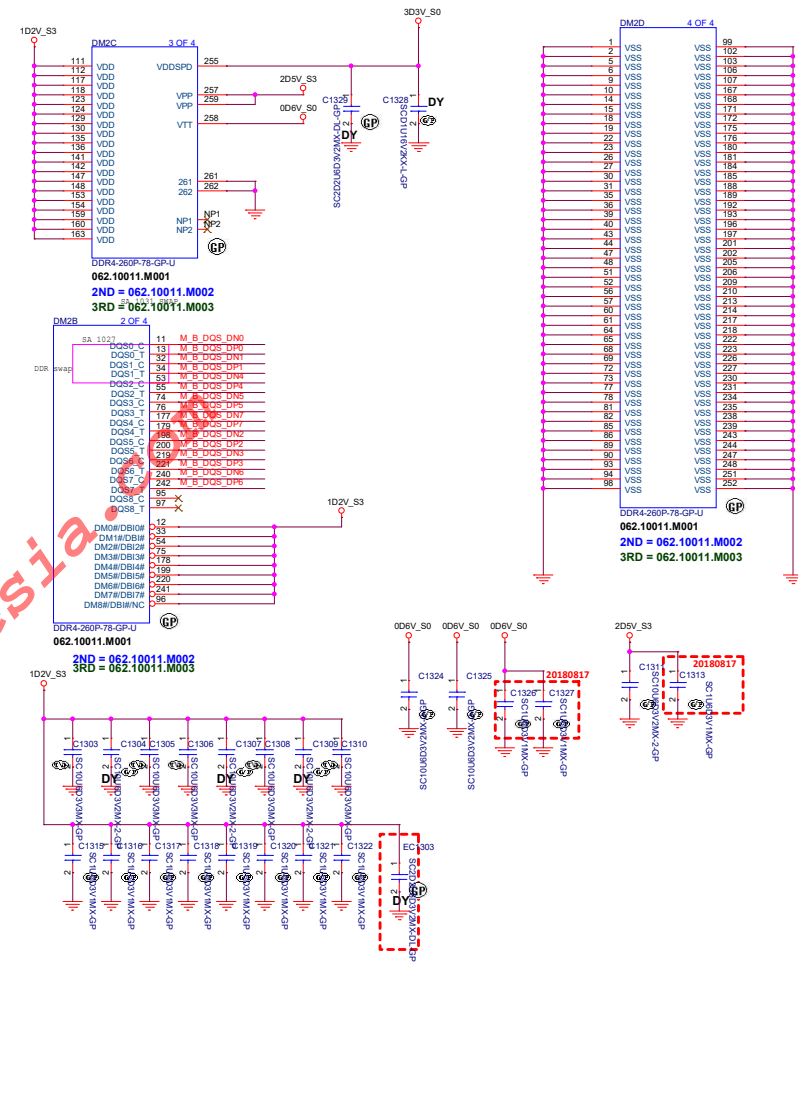
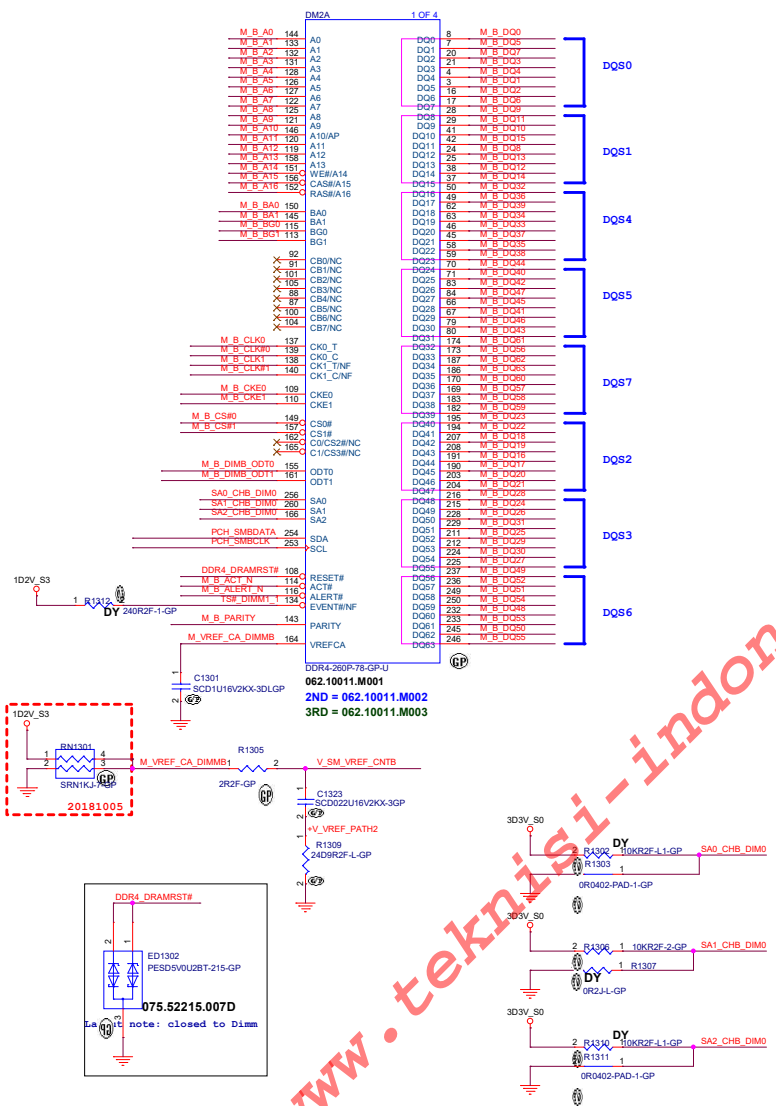
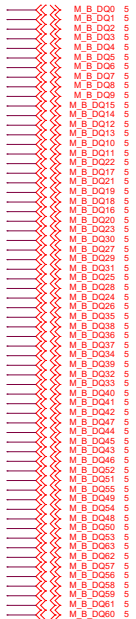
PCH_SMBDATA
PCH_SMBCLK

DDR4_DRAMSTR
M_B_ACT
M_B_ALERT

M_B_PARIT

V_S_M_REF_CN


```



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BOLT L 14 EMMC

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>(Reserved)_SODIMM _SODIMM4</b>					
Size A4		Document Number <b>BOLT WHL</b>			Rev <b>1</b>
Date: Thursday, December 27, 2018			Sheet 14 of 105		

**GFP\_B18**

302V\_B18\_F04

R1302

R1302-GFP

R1302

R1302-GFP

**GFP\_C2**



10348\_R1881

10348\_G1881

10348\_GFP\_C2

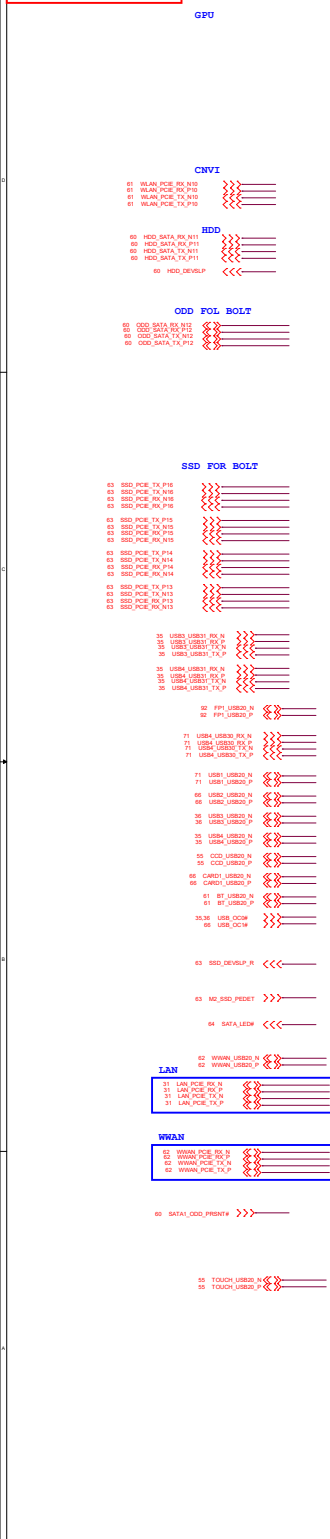
GPP\_80 / HGA\_800 /  
120E\_TK0 / NUCAPU\_800

120E\_VICPWR

RHSIG  
ACROGLO-OP

DW

HGA\_SQOUT



#543016:  
220 nF nominal capacitors are recommended for Gen 3.  
400 nF nominal capacitors are recommended for Gen 2.

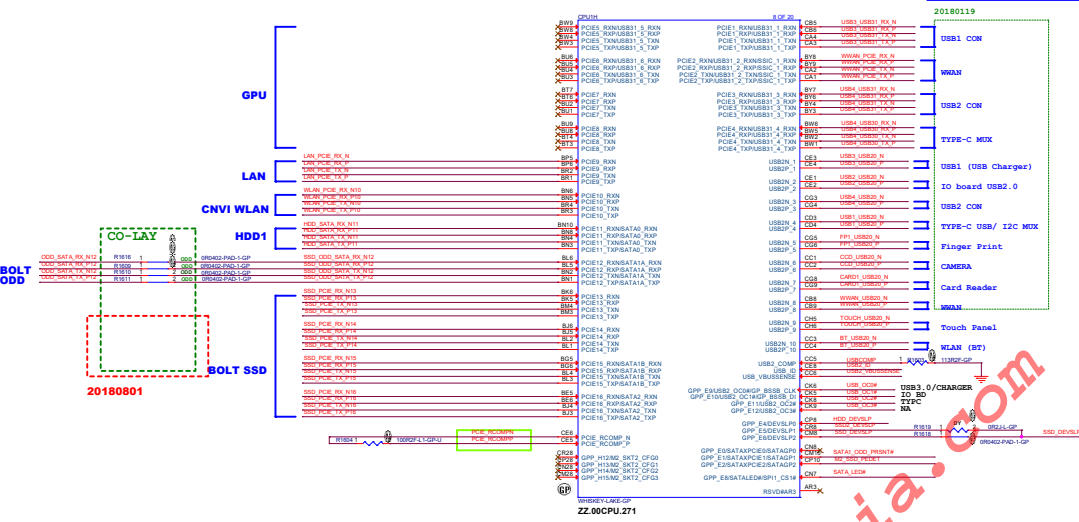


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16	
High Speed I/O (HSIO) Type and Lane	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	GbE	GbE	GbE	SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2	
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes

#### 6.4.1 PCH PCI Express\* Device Down Guidelines

Figure 6-3. PCH PCI Express\* Device Down at 2.5, 5, and 8 GT/s Topology

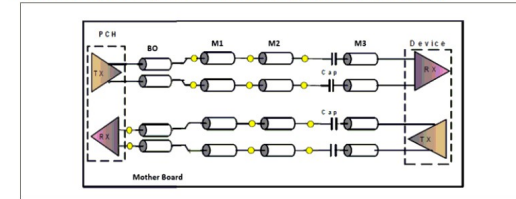


Table 6-6. PCH PCI Express\* Device Down Routing Guidelines (Sheet 1 of 2)

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	BO, M1, M2, M3	MS/SL/DSL	NA	GND	GND	GND
Break-Out Max Length	BO	MS/SL/DSL	mm(mils)	15.2(598.42)	15.2(598.42)	15.2(598.42)
Post-AC Capacitor Max Length	M3	MS	mm(mils)	8(314.96)	8(314.96)	8(314.96)

#543559: The xHCI controller supports USB Debug port on all USB3.0 capable ports.

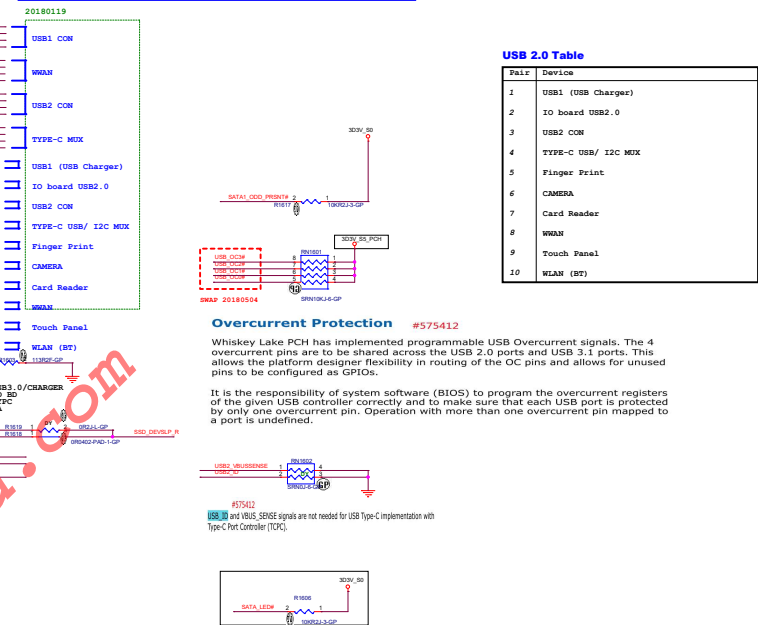


Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DORA SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIe_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on p1g to VSS DDR_RCOMP[1]: 80.6Ω ±1% on p1g to VSS DDR_RCOMP[2]: 162Ω ±1% on p1g to VSS	DDR_RCOMP[0]: 121Ω ±1% on p1g to VSS DDR_RCOMP[1]: 80.6Ω ±1% on p1g to VSS DDR_RCOMP[2]: 100Ω ±1% on p1g to VSS	24.9Ω ±1% to VCCO	49.9Ω ±1% to GND	100Ω ±1% Differential	113Ω ±1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	x	x				
HDMI			x			
DP			x			
eDP			x			
CFG				x		
PCIe					x	
USB2						x

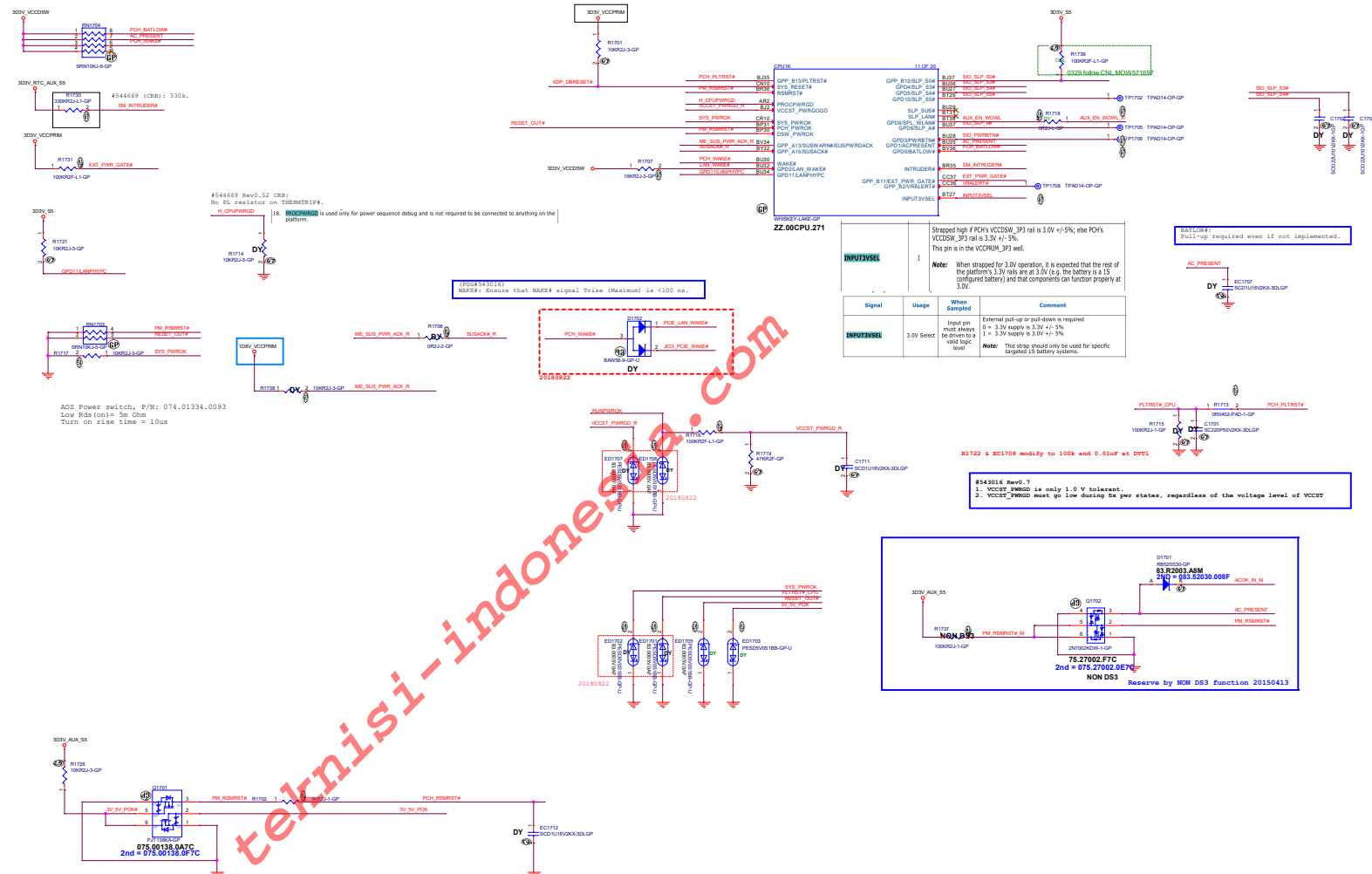
```

24  SYS_PARK          >>> _____
24.30 RESET_OUT9     >>> _____
24.60 RUNPARK        >>> _____
24.645 IN_PCK        >>> _____
24.64 PCH_MASTER#    >>> _____
40.9182 ISO_SLP_SW   >>> _____

40.91 ISO_SLP_SW     <<< _____
40  ISO_SLP_SW       <<< _____
24.61 AIN_EN_WDCH_R  <<< _____
24.615 AIN_WDCH_R    <<< _____
43.64 ACQD_IN_S1     <<< _____
36.31 B1_E1_S2       <<< _____
18  H1_PDRPWRIG2     <<< _____
13 INPUTWDEL        <<< _____

15.2451 JCDI_PCH_WANDEH >>> _____
24.31 PCH_LAN_WANDEH  >>> _____
24.61 PCH_WANDEH      >>> _____

```





---

--	--

BOLT L 14 EMMC

		<b>Wistron Corporation</b> 21F, 8th, Sec. 1, Hsin Tsuei Wld Bldg., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
File			
<b>CPU (LPC/SPI/SMBUS/CLK/CLK)</b>			
Size	DocuMent Number		Rev
A1		<b>BOLT WHL</b>	1
Date:	Thursday, December 27, 2018	Printed	18 of 100



**Main Func = PCH**

```

>>> <<<
<<< >>>
    KB BL LED
65 KB_LED_BD_DET>>>

EDP DMIC
55 DMIC_PCH_CLK>>>
55 DMIC_PCH_DATA>>>

CNVI
61 BT_PCMOUT_CLKREQ0<<<
61 BT_PCMFRM_RSTN<<<

CODEC
27 HDA_SYNC_CODECC<<<
27 HDA_SDOUT_CODECC<<<
27 HDA_BITCLK_CODECC<<<
27 HDA_SDOIN_CPU>>>
27 SPKR<<<

DEBUG PORT
68 ME_FWP_R<<<

STRAP
15 HDA_SDOUT_CPU<<<

24,62 WWAN_DB_DET>>>

LAN CABLE
31 LOM_CABLE_DETECT#>>>

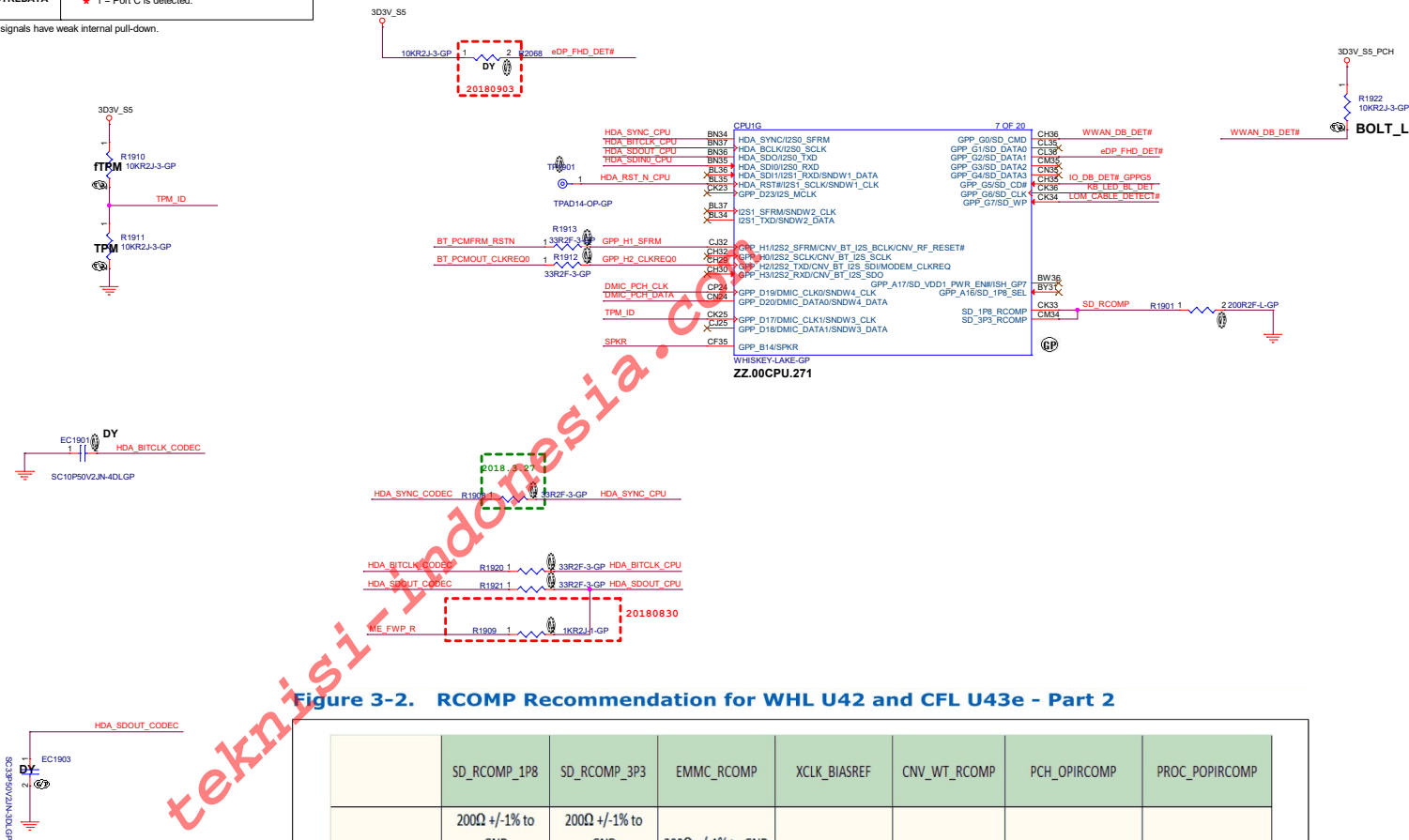
66 IO_DB_DET#_GPGPS<<<

```

**Strap pin:**

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



**Figure 3-2. RCOMP Recommendation for WHL U42 and CFL U43e - Part 2**

	SD_RCOMP_1P8	SD_RCOMP_3P3	EMMC_RCOMP	XCLK_BIASREF	CNV_WT_RCOMP	PCH_OPIRCOMP	PROC_POPIRCOMP
Board Rterm (ohm)	200Ω +/-1% to GND	200Ω +/-1% to GND	200Ω +/-1% to GND	60Ω +/-1% to GND	150Ω +/-1% to GND	49.9Ω +/-1% to GND	49.9Ω +/-1% to GND
	Notes: SD_RCOMP_1P8, SD_RCOMP_3P3 and EMMC_RCOMP can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.						
Board Rdc (ohm)	<0.1	<0.1	<0.1	<0.5	<0.5	<0.2	<0.2
SD3	X	X					
EMMC			X				
POPI						X	X
XTAL				X			
CNV1_DPHY					X		

**BOLT L 14 EMMC**



# Main Func = PCH

61 BLUETOOTH\_EN <<<  
61 WIFI\_RF\_EN <<<

20,64 PWR\_BD\_DET# >>>

15 GPP\_H21 >>>  
15 GPP\_H23 >>>  
15 GPD\_7 >>>

40 GPPC\_H18\_VCCIO\_LPM <<<  
18 PROJECT\_ID0 <<<

## CNvi TX for wifi

61 CNV\_WT\_CLK\_DP >>>  
61 CNV\_WT\_CLK\_DN >>>  
61 CNV\_WT\_DP0 >>>  
61 CNV\_WT\_DN0 >>>  
61 CNV\_WT\_DP1 >>>  
61 CNV\_WT\_DN1 >>>

## CNvi RX for wifi

61 CNV\_WR\_CLK\_DP >>>  
61 CNV\_WR\_CLK\_DN >>>  
61 CNV\_WR\_DP0 >>>  
61 CNV\_WR\_DN0 >>>  
61 CNV\_WR\_DP1 >>>  
61 CNV\_WR\_DN1 >>>

62 WWAN\_BB\_RST# <<<

20,55 LCD\_CBL\_DET# >>>

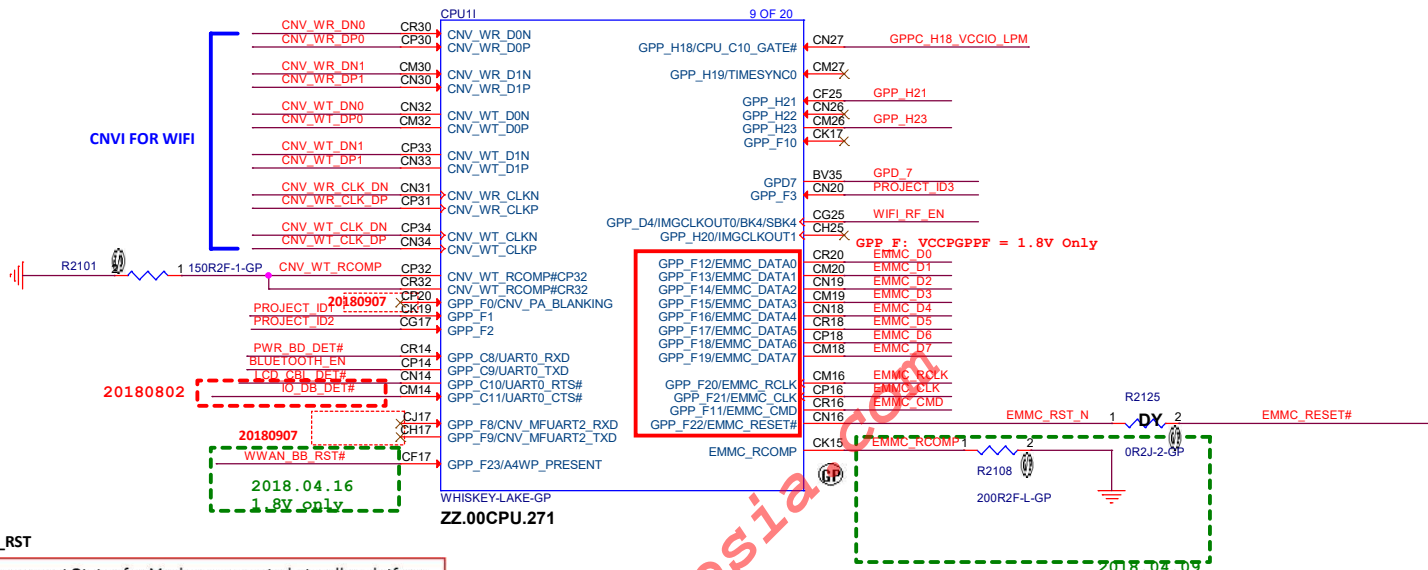
## EMMC

63 EMMC\_D7 <<<  
63 EMMC\_D6 <<<  
63 EMMC\_D5 <<<  
63 EMMC\_D4 <<<  
63 EMMC\_D3 <<<  
63 EMMC\_D2 <<<  
63 EMMC\_D1 <<<  
63 EMMC\_D0 <<<

63 EMMC\_CLK >>>  
63 EMMC\_CMD >>>  
63 EMMC\_RCLK <<<  
63 EMMC\_RESET# <<<

## IO BD DET

66 IO\_DB\_DET# <<<



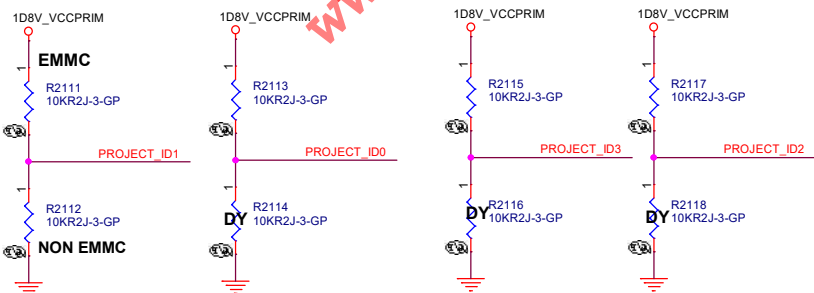
## WWAN\_BB\_RST

### Power Management States for Modern connected standby platform

System States	USB device States	PCIe device States	PCIe Link States	PERST#	PEWAKEN	CLKREQ#	BS_RESET#	Notes
S0	D0	D0	L0, L1.2	H	H	L0 : L1.2 : H	H	
	D2	D3cold	L2	L	H	H	H	
S0ix	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem
S4	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	
S5	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem

### PROJECT\_ID[1:0] 01: 7000 Series

### PROJECT\_ID[3:2] 11: Inspiron



<Core Design>



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Title

**CPU (POWER1)**

Size

Document Number

**BOLT WHL**

Rev

**1**

Date: Thursday, December 27, 2018

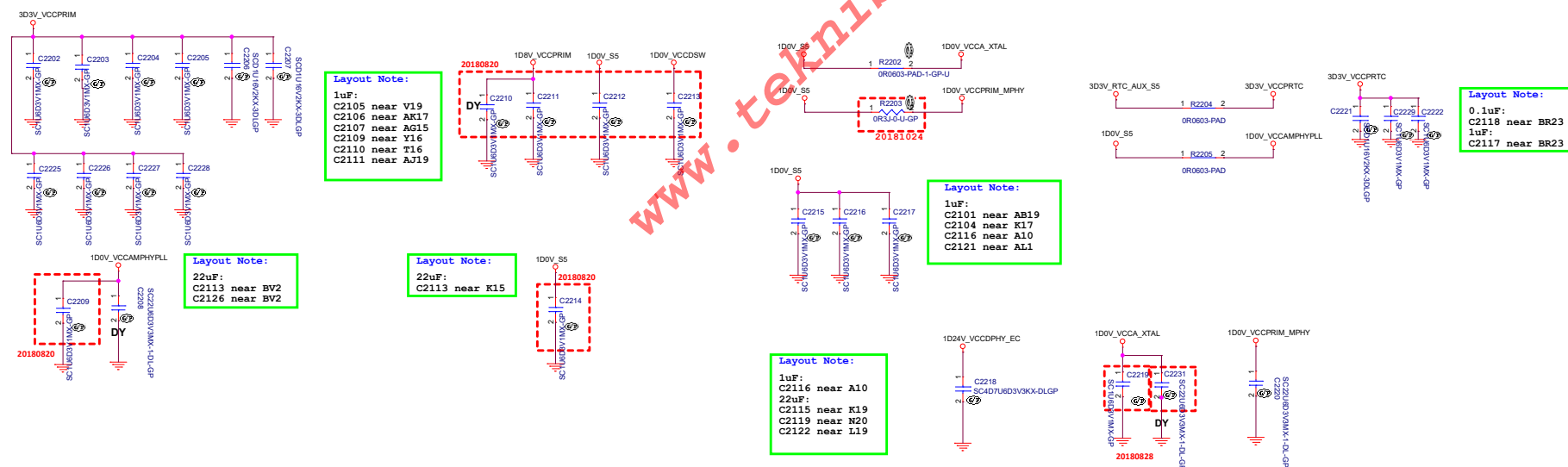
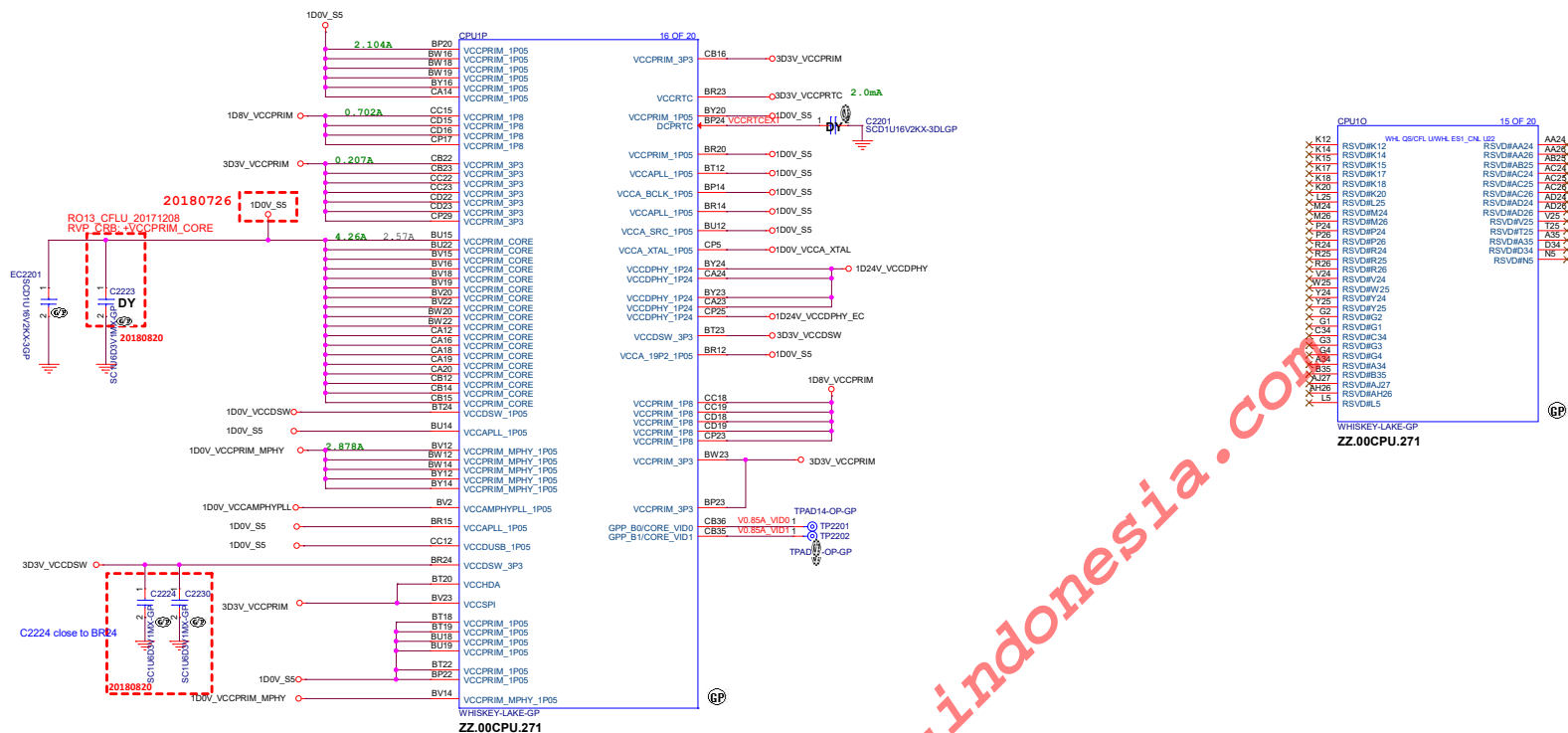
Sheet

21

of

105

**Main Func = PCH**

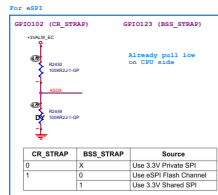
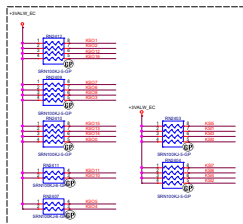
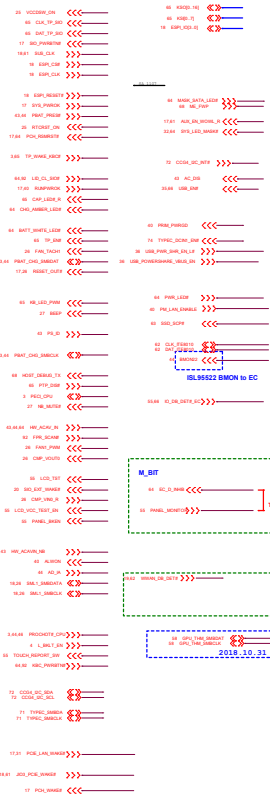


CPU1R 18 OF 20

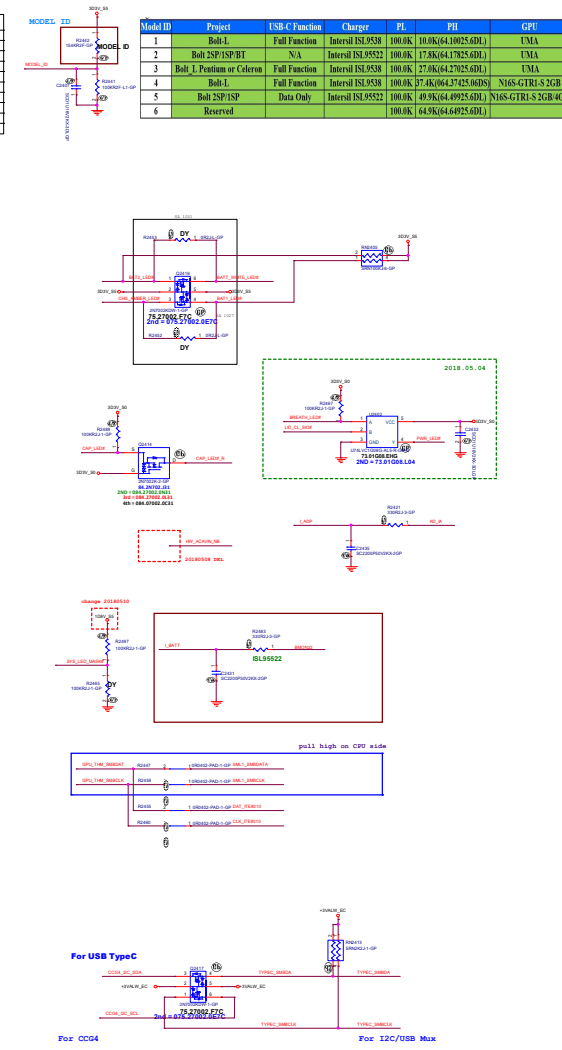
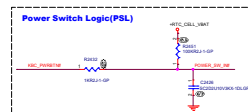
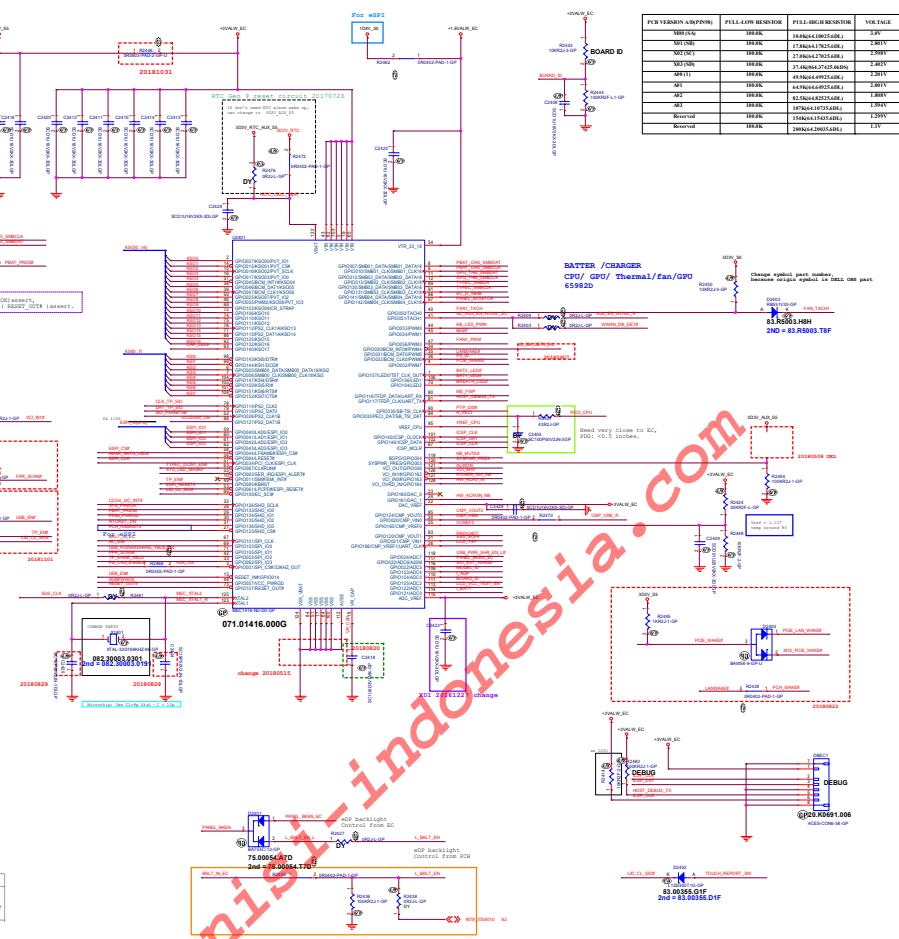
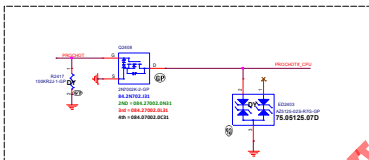
WHISKEY-LAKE-GP  
ZZ.00CPU.271

ZZ.00CPU.271ZZ.00CPU.271

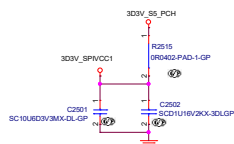
Main Func = KBC



CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use vSPI Flash Channel
1	1	Use 3.3V Shared SPI

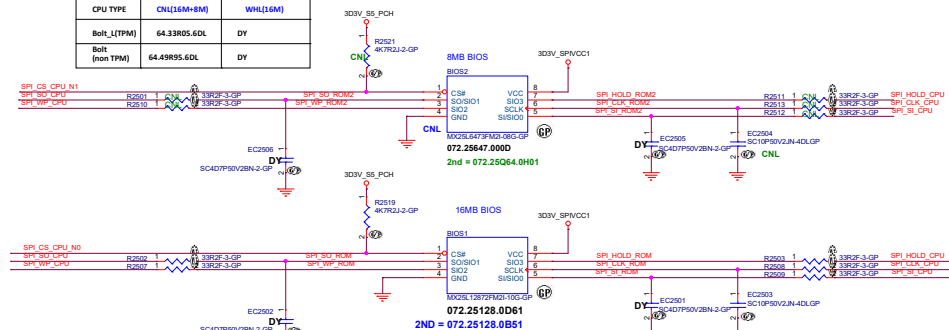


18	SPI_CS_CPU_N1	>>>
18	SPI_CS_CPU_N0	>>>
15,18	SPI_HOLD_CPU	<<<
24	RTCRST_ON	>>>
53	3V_5V_DSW_OK	<<<
18,91	SPI_SO_CPU	<<<
15,18	SPI_WP_CPU	<<<
18,91	SPI_CLK_CPU	>>>
15,18,91	SPI_SI_CPU	>>>
15,20	RDC_DET#	<<<
24	VCCDSW_ON	>>>
17,40,45	3V_5V_POK	>>>

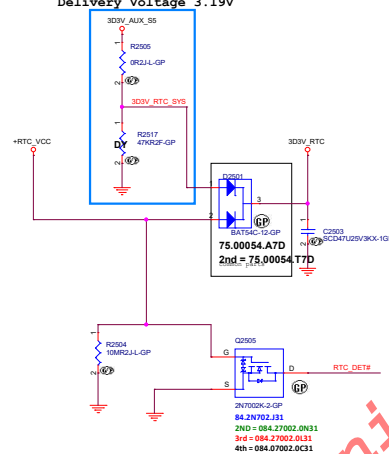


R2502/R2507/R2503/R2508/R2509		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	64.49R95.6DL	63.R0034.L0L

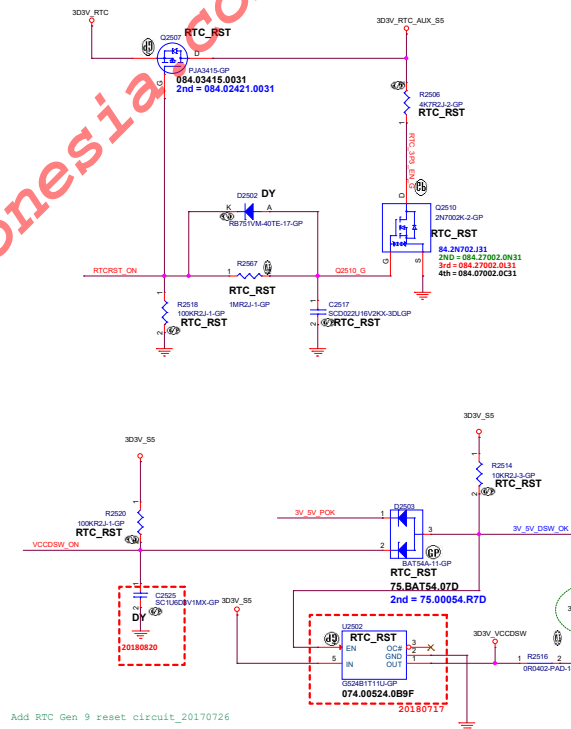
R2501/R2510/R2511/R2513/R2512		
CPU TYPE	CN1[16M+8M]	WHL[16M]
Bolt_L(TPM)	64.33R05.6DL	DY
Bolt (non TPM)	64.49R95.6DL	DY



Delivery Voltage 3.19V



On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW\_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



Add RTC Gen 9 reset circuit 20170726

**BOLT L 14 EMMC**

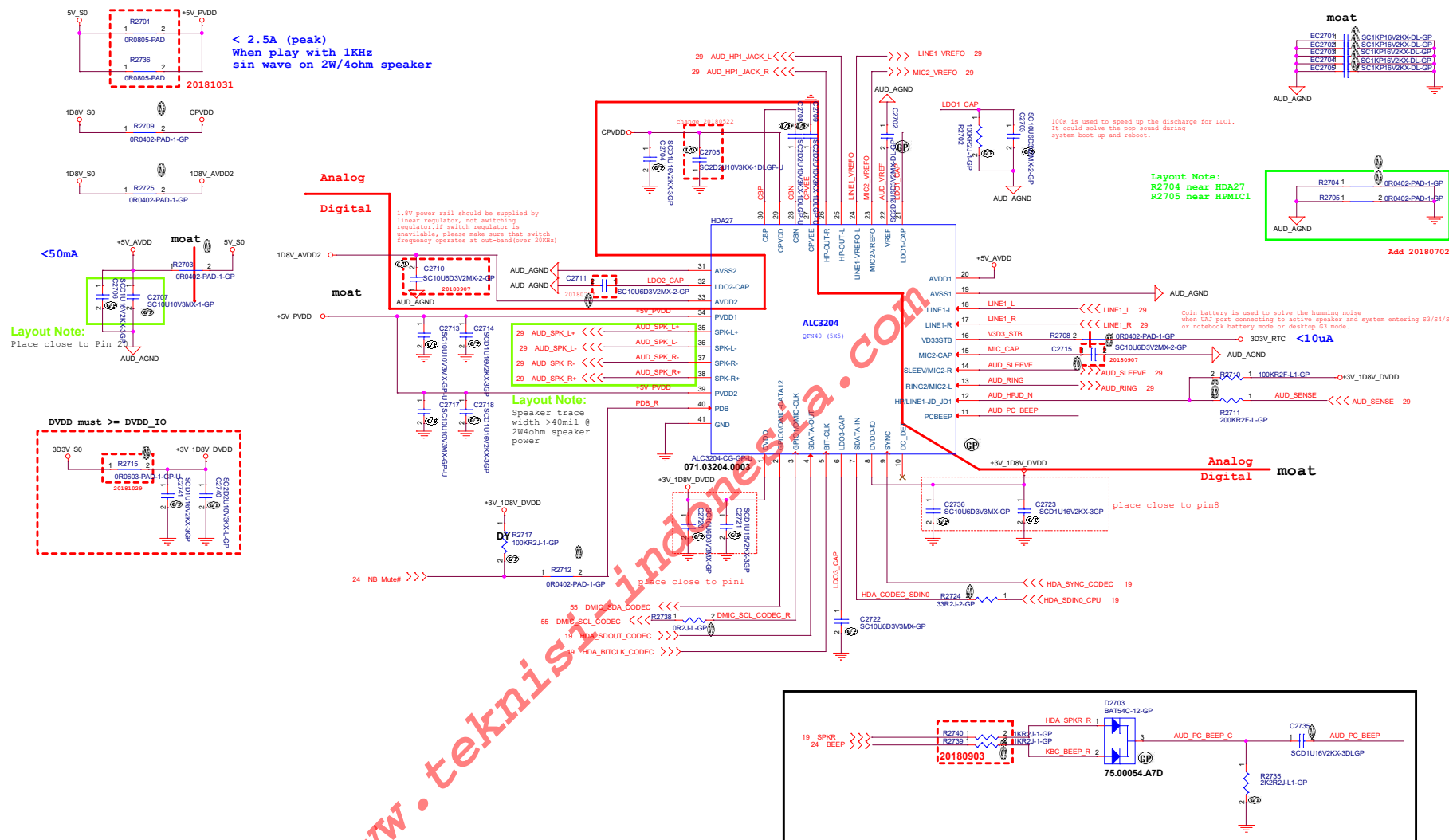


File		<b>Flash/RTC</b>		Rev	1
Size Custom	Document Number				
		<b>BOLT WHL</b>			
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**Main Func = Audio**



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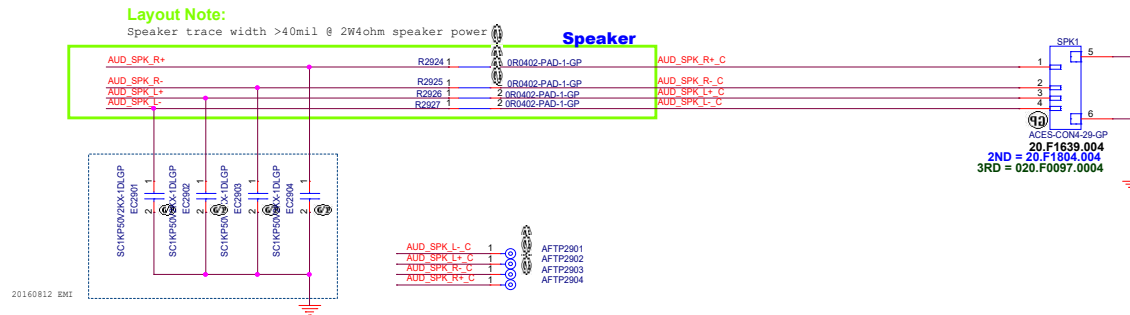
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Title <b>(Reserved)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
Date: Thursday, December 27, 2018		Sheet 28 of	105

# Main Func = Audio

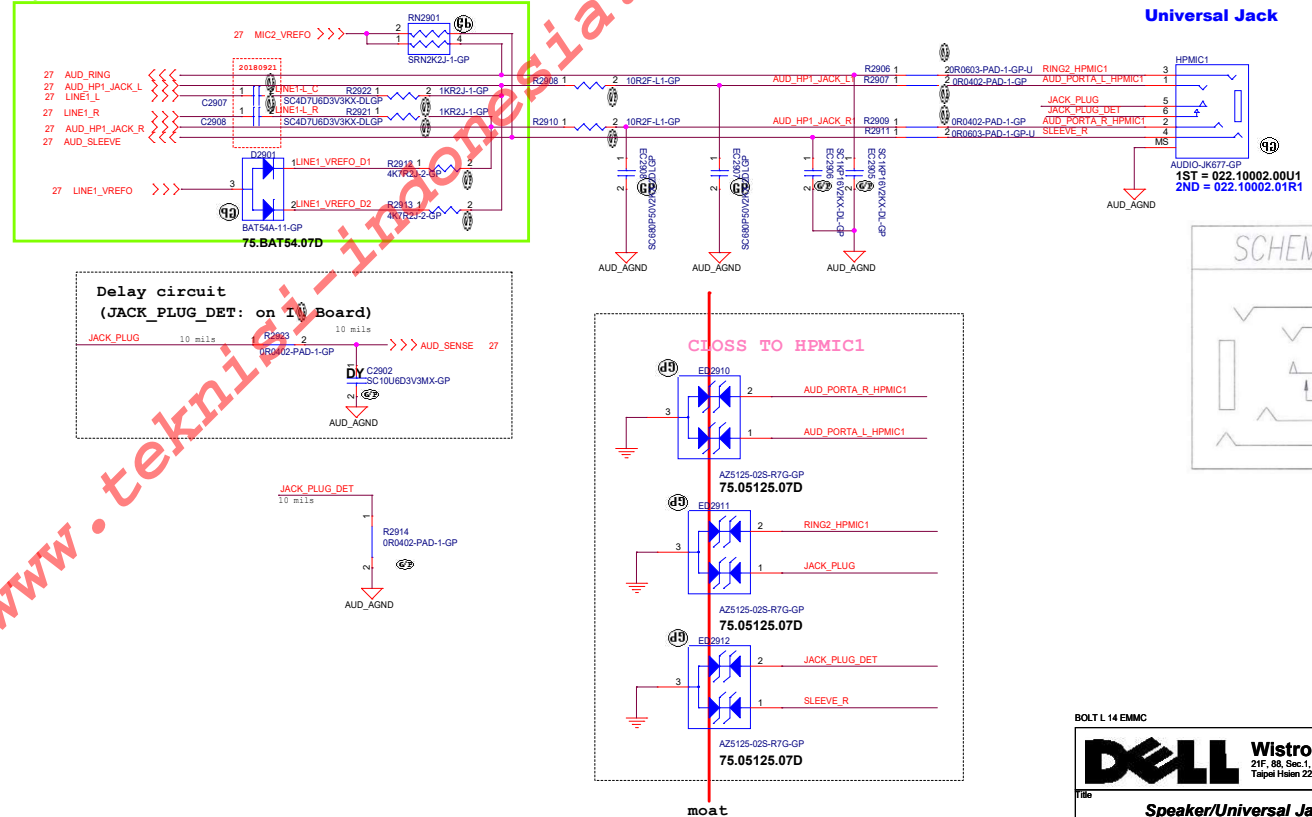
## SPEAKER

27 AUD\_SPK\_R+ >>>  
27 AUD\_SPK\_R- >>>  
27 AUD\_SPK\_L+ >>>  
27 AUD\_SPK\_L- >>>



## Audio Jack

**Layout Note:** Should be placed nearby codec IC (HDA27).



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Title			
<b><i>Speaker/Universal Jack</i></b>			
Size	Document Number	Rev	
Custom	<b>BOLT WHL</b>	<b>1</b>	
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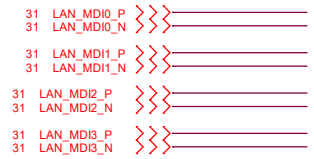
Sheet 30 of 105



Main Func = LAN

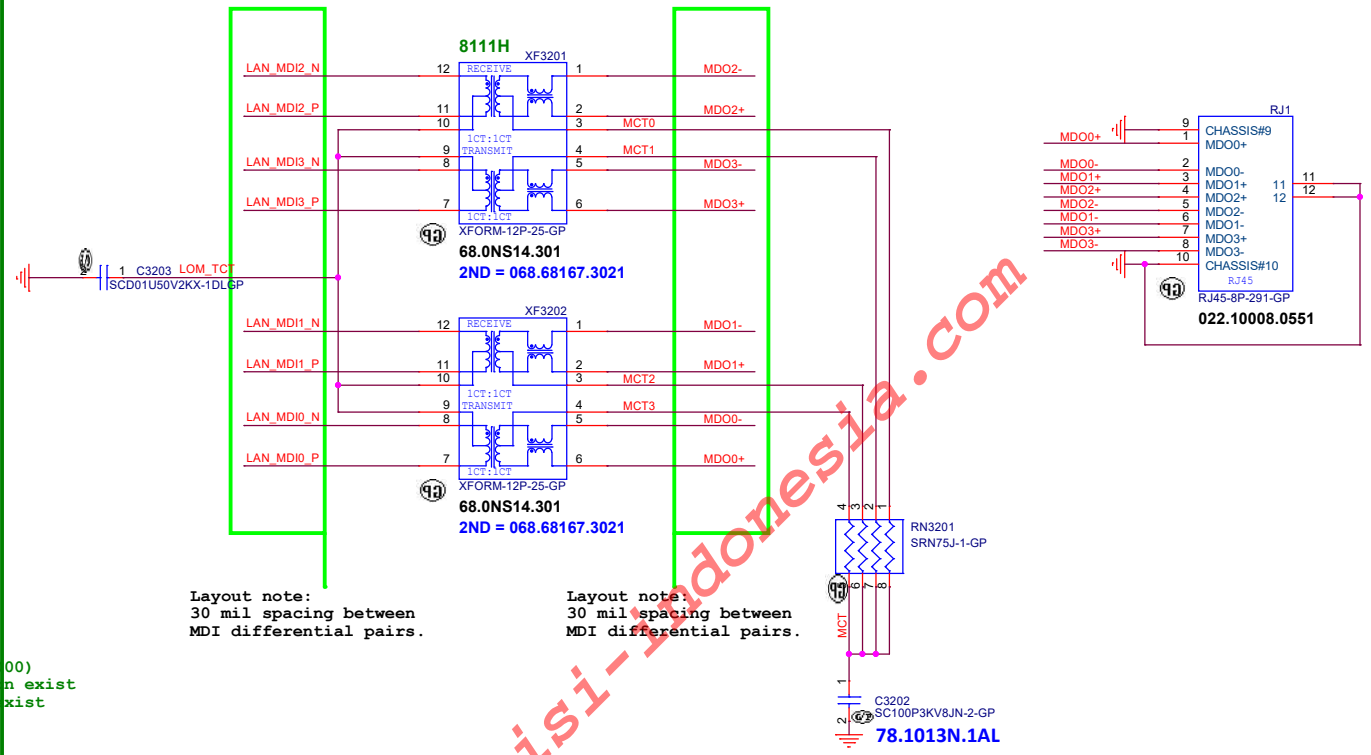
LAN TransFormer (10/100/1000M & 10/100M co-lay)

MDI

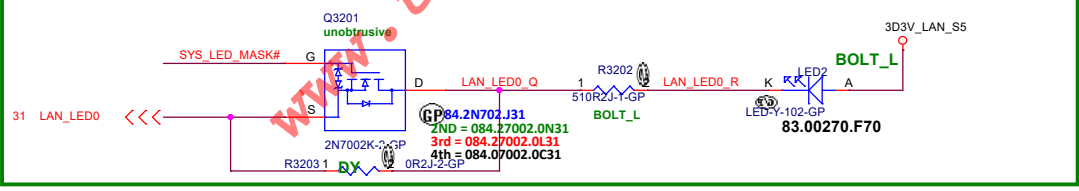


24.64 SYS\_LED\_MASK# >>>

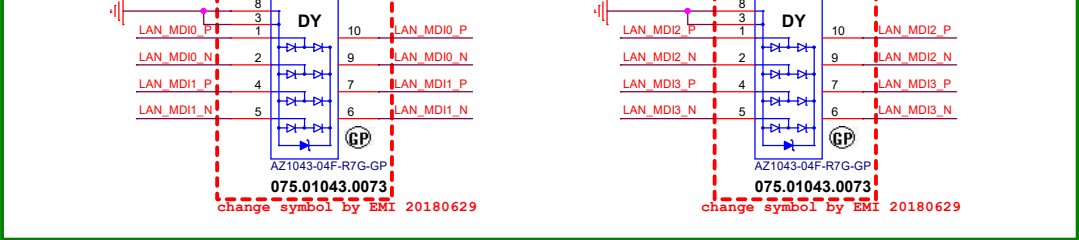
Green LED Status:  
Blinking:Data transmit (10/100/1000)  
Always Turn On: Network Connection exist  
Turn Off: No network connection exist



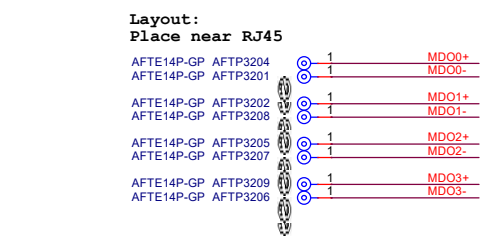
LED



LED



TEST PAD



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**DELL**

XFOM&RJ45

Size A3 Document Number BOLT WHL Rev 1

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Title

**USB2.0 CONN**

Size

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Date: Thursday, December 27, 2018

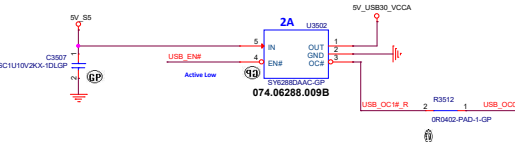
Sheet 34 of 105

Main Func = USB3.0

## USB Power Switch Enable



## USB Power Switch

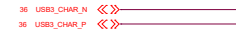


## USB Power Sharing



31 瓦 風扇 (W) ≥ 1Q & 0Q													
型別	電壓 (V)	電流 (A)	風速 (m/s)	轉速 (RPM)	所接電壓					JUMPER (J2)		JUMPER (J3)	
					標準 1% 電流 (A)	D2045 (A)	F10 (A)	G10 (A)	J45 (A)	I2 (A)	F (A)	J3 (A)	F (A)
RT101 (R045)	$\frac{1}{10}$ 2V	25V	50V	300	±50V	470Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	0.5A 1A	500Ω Max		
RT102 (R045)	$\frac{1}{10}$ 5V	50V	100V	600	±50V	470Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	1A	500Ω Max		
RT103 (R045)	$\frac{1}{10}$ 10V	100V	200V	1200	±50V	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	1A	2A	500Ω Max	
RT104 (R045)	$\frac{1}{10}$ 15V	150V	300V	1500	±50V	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	1A	2A	500Ω Max	
RT105 (R045)	$\frac{1}{10}$ 20V	200V	400V	1800	±50V	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	2A	500Ω Max		
RT106 (R045)	$\frac{1}{10}$ 25V	250V	500V	2000	±50V	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	3A	500Ω Max		
RT107 (R045)	$\frac{1}{10}$ 30V	300V	600V	2200	±50V	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	100Ω ±10% (A)	3A	500Ω Max		

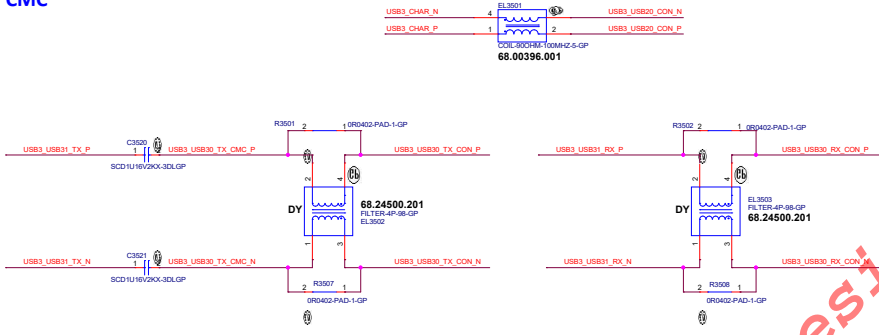
## USB2.0 from USB Charger



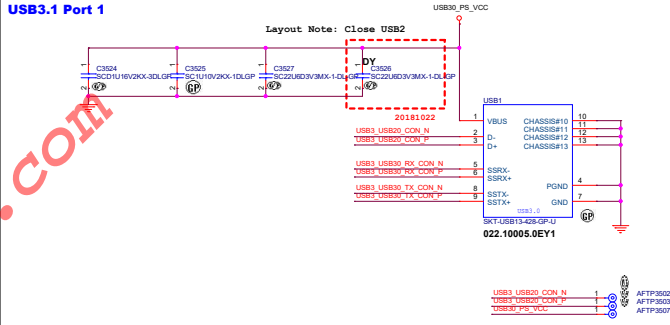
## USB3.1



## CMC



**USB-A Connector**  
**USB3.1 Port 1**



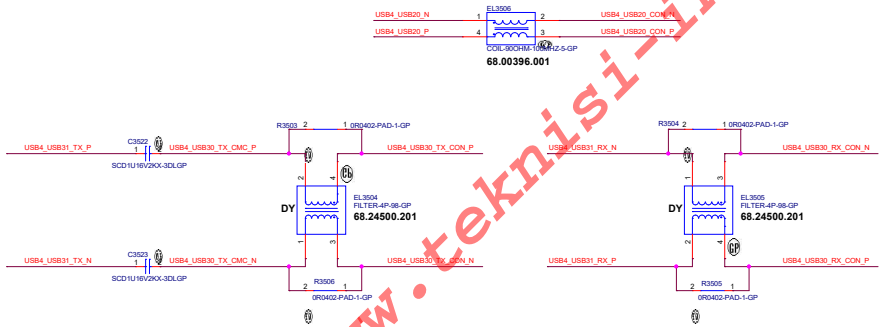
## USB2.0



## USB3.1

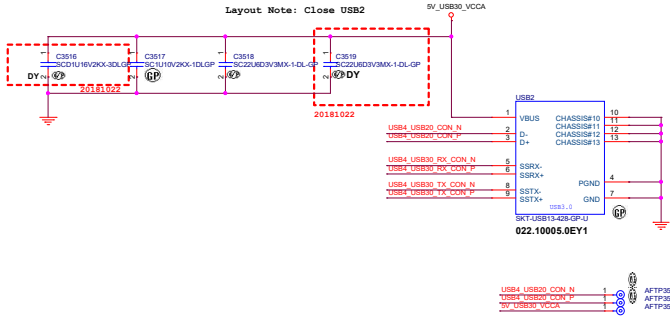


## CMC

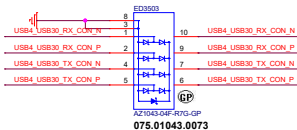


### USB-A Connector

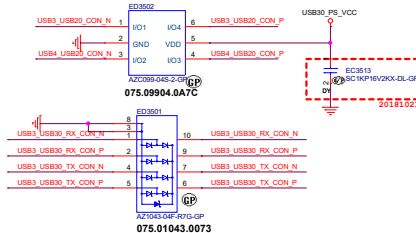
#### USB3.1 Port 2



## ESD FOR PORT1

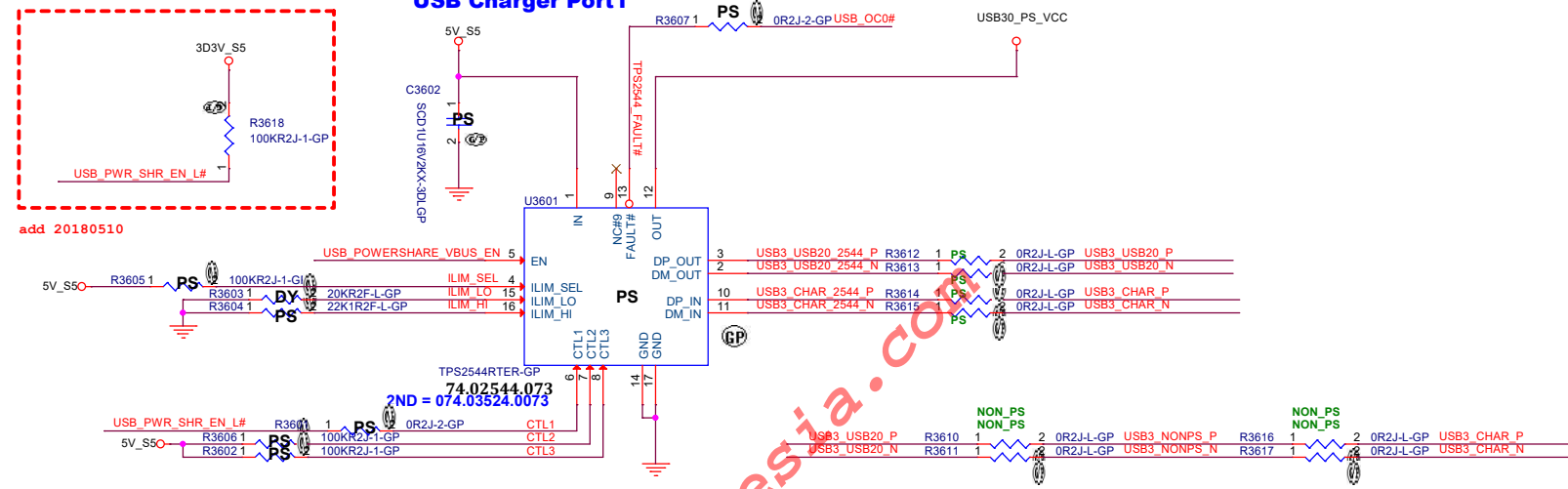


## ESD FOR PORT2



Main Func = USB Charger

Reserved  
USB Charger Port1



35 USB3\_CHAR\_P <<<=====

35 USB3\_CHAR\_N <<<=====

16 USB3\_USB20\_P <<<=====

16 USB3\_USB20\_N <<<=====

24 USB\_POWERSHARE\_VBUS\_EN >>>=====

24 USB\_PWR\_SHR\_EN\_L# >>>=====

16,35 USB\_OC0# <<<=====


Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_vp} (mA) = \frac{50,500}{(R_{ILIM\_XX} (k\Omega) + 0.1)}$$

R<sub>ILIM,XX</sub> corresponds to either R<sub>ILIM\_HI</sub> or R<sub>ILIM\_LO</sub> as appropriate.

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Title

**USB Charger**

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Title			
<b>USB3.0 PORT</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
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Date: Thursday, December 27, 2018		Sheet 41 of	105

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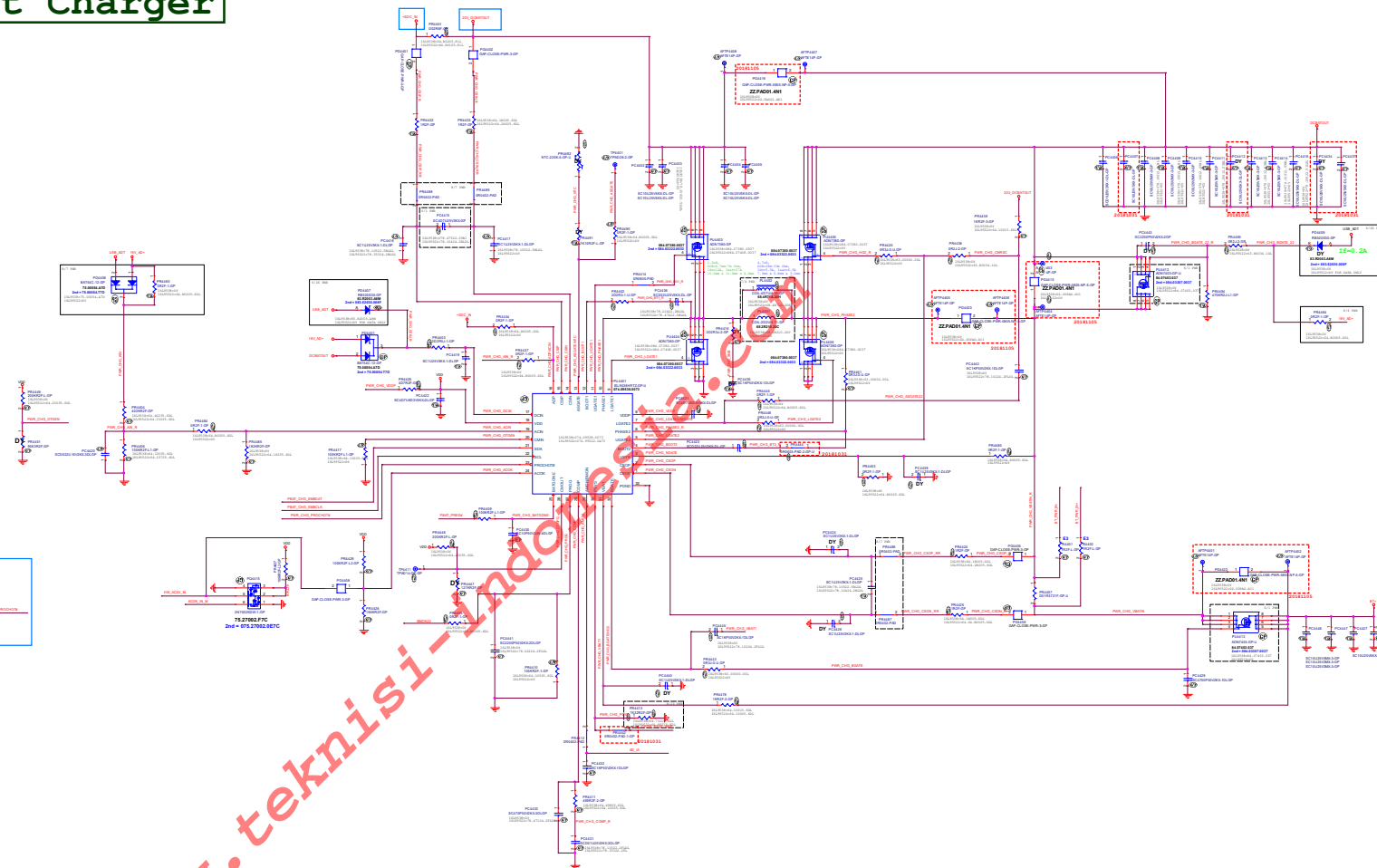
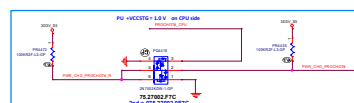
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Title <b>Connected_Standby(2/2)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
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## ISL9538 Buck-Boost Charger

[illegible][illegible]

PROG. REMARKS (a)	TYPE MIN	MAX	CELL	DEFAULT SUPPORTING FUNCTIONS	Autonomous charging	DEFAULT ACQUIES # (b)
0	1	2		723000	Yes	2.00
8.45				723000	Yes	1.5
10.7				18000	Yes	1.5
25.0				18000	Yes	0.675
26.0				723000	Yes	0.675
43.2			2	723000	Yes	1.5
45.5				723000	Yes	0.675
61.5				18000	Yes	0.675
71.5				18000	Yes	1.5
82.6				723000	Yes	1.5
93.4				723000	Yes	0.675
105			3	723000	Yes	1.5
123				18000	Yes	1.5
140				18000	Yes	0.675
157				723000	Yes	1.5
176				723000	Yes	2.5
195				723000	Yes	1.5
215				723000	Yes	0.675
237				18000	Yes	0.675
257				723000	Yes	1.5
316				723000	Yes	0.675

Table 11. Prog Pin Programming Options			
Prog-GND Resistance (kΩ)	Charger Type	Current Sense Resistor Value	Default # of Battery Cells in Series
Type (1% Standard Resistor)			
22.6	NTDC	$R_{CS} = 1\Omega$	4
38.3		$R_{CS} = 10m\Omega$	2
		$R_{CS} = 100m\Omega$	2
		$R_{CS} = 1\Omega$	3
		$R_{CS} = 10m\Omega$	2
69.8	HPB	$R_{CS} = 1\Omega$	3
106		$R_{CS} = 10m\Omega$	2
150		$R_{CS} = 100m\Omega$	2
182		$R_{CS} = 1\Omega$	3
		$R_{CS} = 10m\Omega$	2
215		$R_{CS} = R_{CS} + 21$	3
237		$R_{CS} = 50m\Omega$	2
269		$R_{CS} = 10m\Omega$	3



48 PWR\_VCC0T\_BEN1 >>>  
48 PWR\_VCC0T\_BEN2 >>>

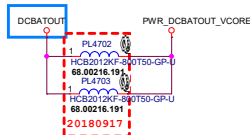
- 32A4 PROCHOTN\_GD
- 1 VCCORE\_SENSE
- 2 VCCORE\_SENSE
- 3 PWR\_VCC0T\_BEN1
- 4 PWR\_VCC0T\_BEN2
- 5 PWR\_VCC0T\_BEN3
- 6 PWR\_VCC0T\_BEN4
- 7 SBE\_ALERTN\_CPU
- 8 SBE\_ALERTN\_CPU
- 9 SBE\_ALERTN\_CPU
- 10 PWR\_VCC0T\_BEN1
- 11 PWR\_VCC0T\_BEN2
- 12 PWR\_VCC0T\_BEN3
- 13 PWR\_VCC0T\_BEN4
- 14 PWR\_VCC0T\_BEN5
- 15 PWR\_VCC0T\_BEN6
- 16 PWR\_VCC0T\_BEN7
- 17 PWR\_VCC0T\_BEN8
- 18 PWR\_VCC0T\_BEN9
- 19 PWR\_VCC0T\_BEN10
- 20 PWR\_VCC0T\_BEN11
- 21 PWR\_VCC0T\_BEN12
- 22 PWR\_VCC0T\_BEN13
- 23 PWR\_VCC0T\_BEN14
- 24 PWR\_VCC0T\_BEN15
- 25 PWR\_VCC0T\_BEN16
- 26 PWR\_VCC0T\_BEN17
- 27 PWR\_VCC0T\_BEN18
- 28 PWR\_VCC0T\_BEN19
- 29 PWR\_VCC0T\_BEN20
- 30 PWR\_VCC0T\_BEN21
- 31 PWR\_VCC0T\_BEN22
- 32 PWR\_VCC0T\_BEN23
- 33 PWR\_VCC0T\_BEN24
- 34 PWR\_VCC0T\_BEN25
- 35 PWR\_VCC0T\_BEN26
- 36 PWR\_VCC0T\_BEN27
- 37 PWR\_VCC0T\_BEN28
- 38 PWR\_VCC0T\_BEN29
- 39 PWR\_VCC0T\_BEN30
- 40 PWR\_VCC0T\_BEN31
- 41 PWR\_VCC0T\_BEN32
- 42 PWR\_VCC0T\_BEN33
- 43 PWR\_VCC0T\_BEN34
- 44 CHGR\_PSRV\_RAMP

	U22	U42	
PC4614	330P (78.33124.2FLDL)	470p (78.47124.2FLDL)	2017/04/25
PC4618	33P (78.10224.2FLDL)	470p (78.47124.2FLDL)	
PC4625	DY	0.022u (78.22321.2FLDL)	
PC4626	DY	0.022u (78.22321.2FLDL)	2017/02/21
PR4669	DY	DY	
PR4670	1K (64.10015.6DL)	DY	2018/04/27
PR4642	357 (64.35705.6DL)	523 (64.52305.6DL)	
PC4630	47nF (078.47322.02FD)	47nF (078.47322.02FD)	2018/04/27
PC4628	22nF (78.22321.2FLDL)	22nF (78.22321.2FLDL)	
PC4654	0.022uF (78.22321.2FLDL)	0.022uF (78.22321.2FLDL)	2018/04/27
PC4653	DY	47nF (078.47322.02FD)	
PR4633	1.54K (64.15415.6DL)	2.55K (64.25515.6DL)	2018/04/27
PR4608	90.9K (64.90925.6DL)	100K (64.10035.6DL)	

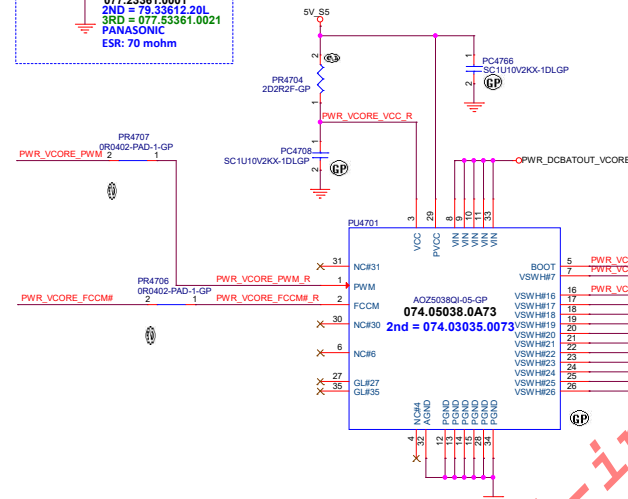
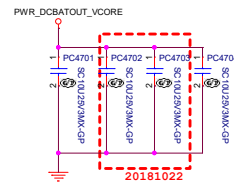
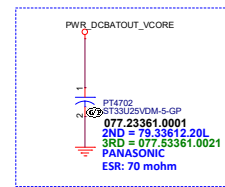
WHL U42\_15W  
VCCORE Icc(max)=70A TDC=48 A  
VCCGT Icc(max)=31A TDC=18 A  
VCCSA Icc(max)=6A TDC=4A

# Main Func = CPU\_CORE

46 PWR\_VCORE\_PWM >>>  
46 PWR\_VCORE\_FCCM <<<  
46 PWR\_VCORE\_ISUMP <<<  
46 PWR\_VCORE\_ISUMN <<<

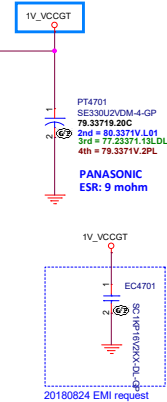


For acoustic noise



CYNTREC 7.3\*6.8\*3mm  
DCR: 0.9m Ohm +/-7%  
Idc: 35A, Isat: 41A

WHL\_U42\_15W  
Icc(max)=31A  
TDC=18A



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<Core Design>





(Blanking)

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BOLT L 14 EMMC



**Wistron Corporation**

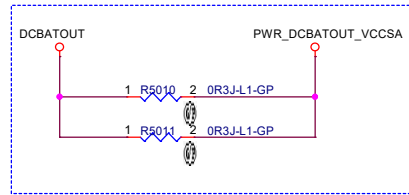
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **NCP81210MN\_CPU\_VCCGTUS**

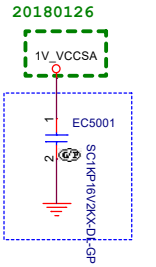
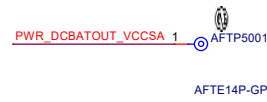
Size A4	Document Number <b>BOLT WHL</b>	Rev <b>1</b>
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Date: Thursday, December 27, 2018 Sheet 49 of 105

**Main Func = CPU\_CORE**



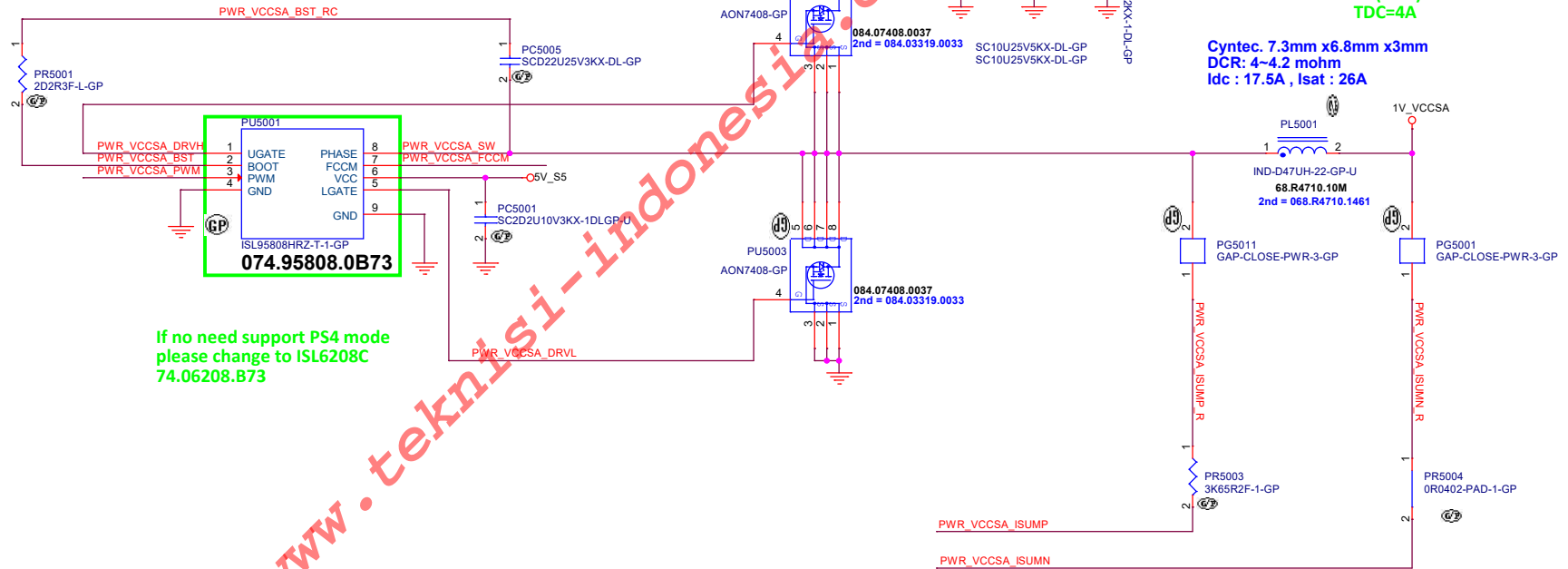
Bolt 20180412 E3 support



20180824 EMI request

WHL\_U42\_15W  
Icc(max)=6A  
TDC=4A

Cyntec. 7.3mm x6.8mm x3mm  
DCR: 4~4.2 mohm  
Idc : 17.5A , Isat : 26A



If no need support PS4 mode  
please change to ISL6208C  
74.06208.B73

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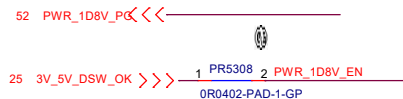
<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>VCCSA</b>			
Size A3	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
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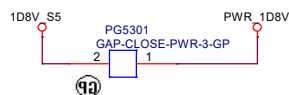
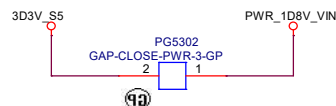


OFFPAGE

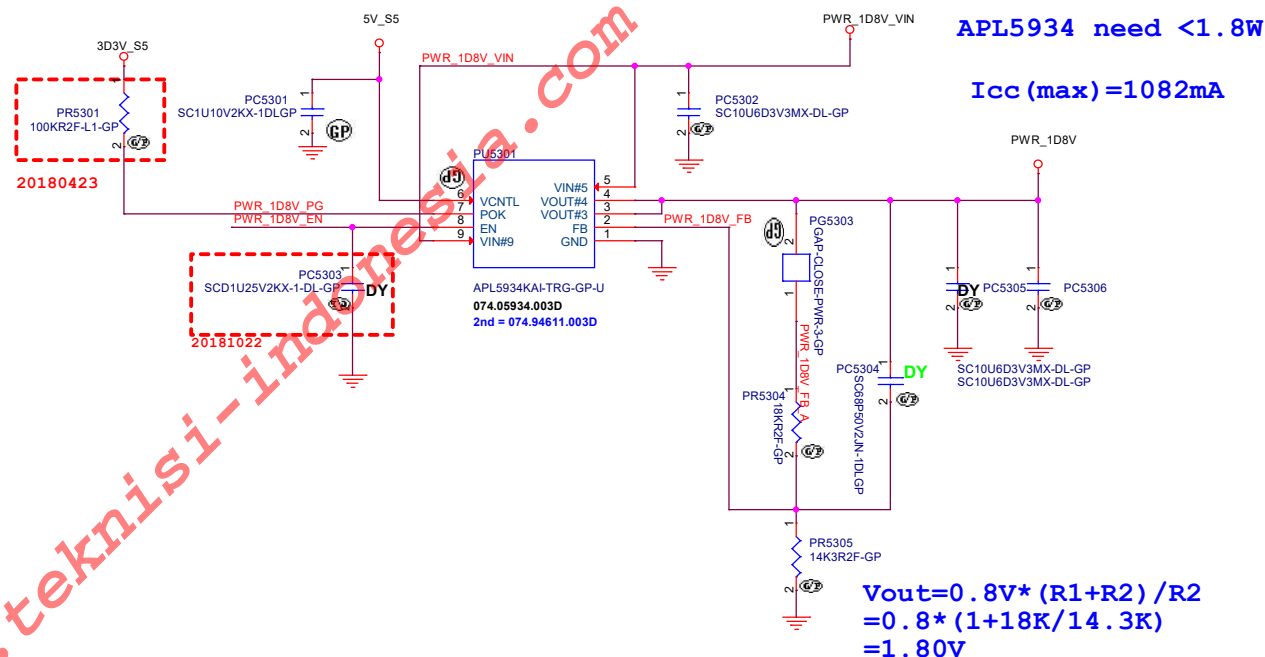
Main Func = 1D8V



OFFPAGE\_GAP



# APL5934 for 1D8V



BOLT L 14 EMMC




**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			1D8V
Size	Document Number	Rev	
A3	BOLT WHL	1	
Date:	Thursday, December 27, 2018	Sheet	53 of 105

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A2	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
Date: Thursday, December 27, 2018      Sheet 54 of 105			

# Main Func = LCD

# INVERTER POWER

# LCDVDD

# Brightness

# EC (BIST MODE)

# Main Func = CAMERA

# IR LED POWER

# Main Func = Touch panel

# TOUCH PANEL POWER

# LCD\_CBL\_DET#

# IR\_CAM\_DET#

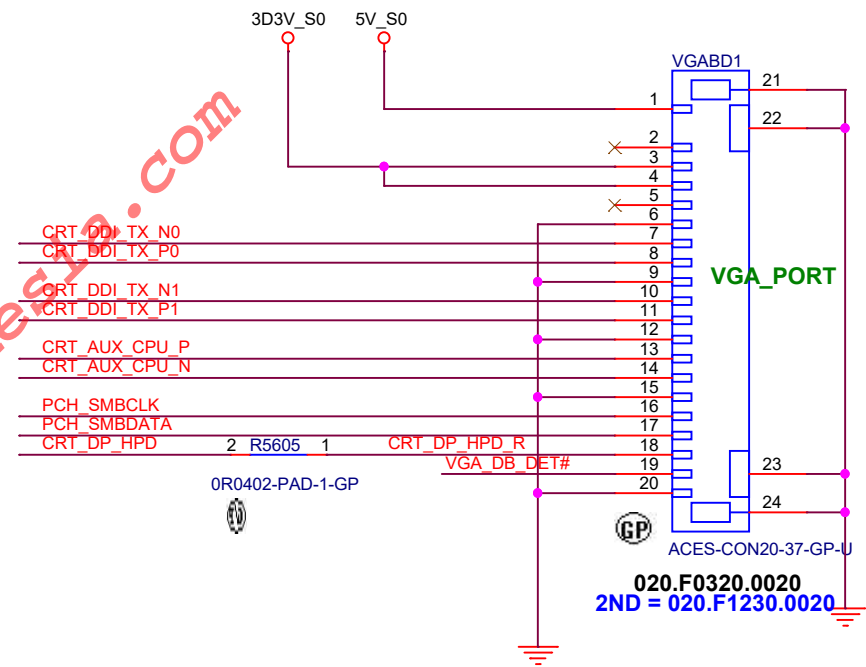
# TOUCH\_LIC\_DET#

# PANEL\_PWRGD CIRCUIT

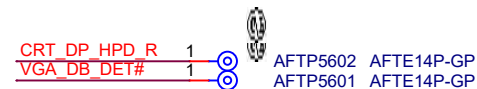


Main Func = CRT

58 CRT\_DDI\_TX\_N0 >>>  
58 CRT\_DDI\_TX\_P0 >>>  
58 CRT\_DDI\_TX\_N1 >>>  
58 CRT\_DDI\_TX\_P1 >>>  
58 CRT\_AUX\_CPU\_P >>>  
58 CRT\_AUX\_CPU\_N >>>  
12,13,18,70 PCH\_SMBCLK <<<  
12,13,18,70 PCH\_SMBDATA <<<  
58 CRT\_DP\_HPD <<<  
20 VGA\_DB\_DET# <<<



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<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CRT</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
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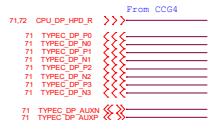


# Main Func = DP Demux

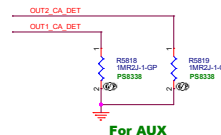
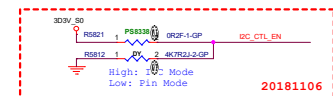
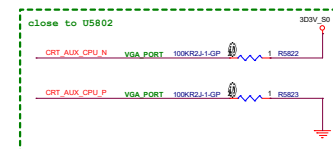
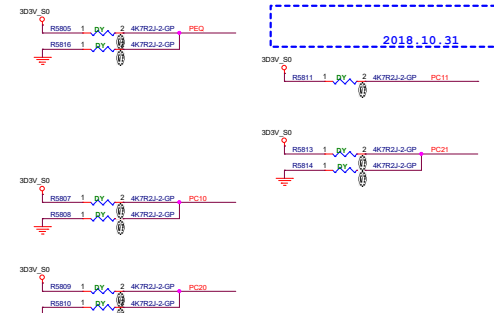
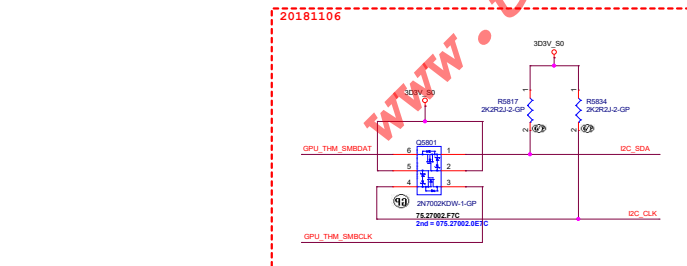
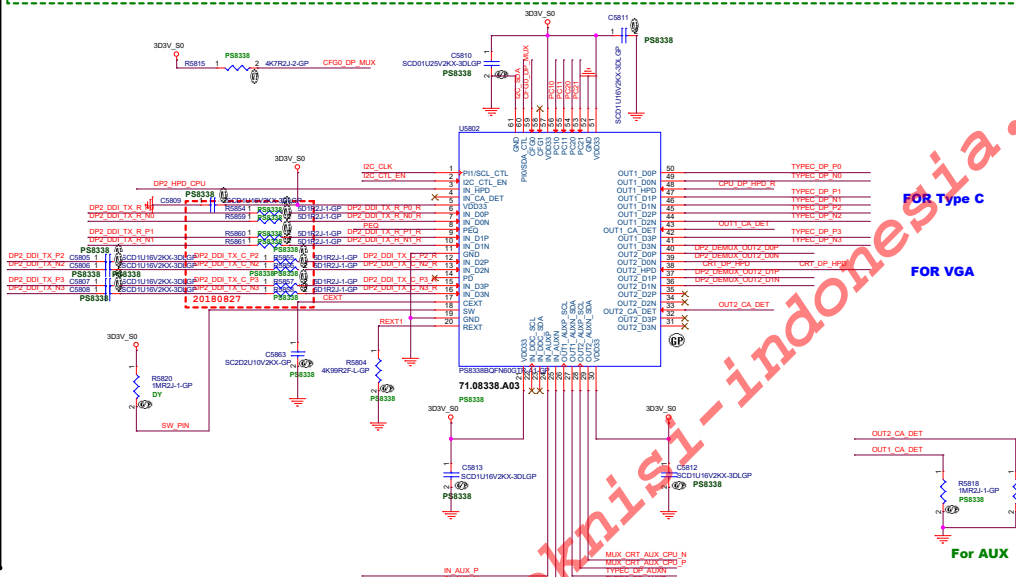
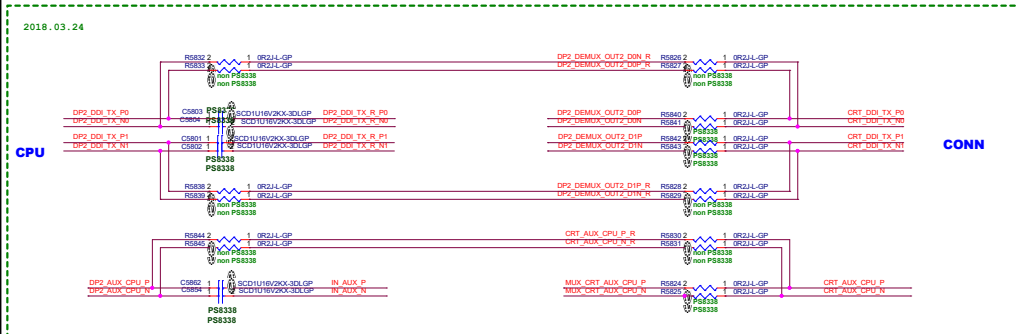
## CPU DP to DP De-MUX



## FOR Type C



## FOR VGA



SW	I/O	Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):		
SW = L: Port1 is selected (default)		
SW = H: Port2 is selected		
For Automatic Switching Mode (CFG0 = H):		
SW = L: Port1 has higher priority when both ports are plugged (default)		
SW = H: Port2 has higher priority when both ports are plugged		
Overwritten by I2C register in I2C Control Mode		

BOLT L 14 EMMC


**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Vda Rd., Hsinchu, Taiwan 30001, Taiwan, R.O.C.  
**DP De-MUX**  
BOLT WHL  
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Rev  
1

(Blanking)

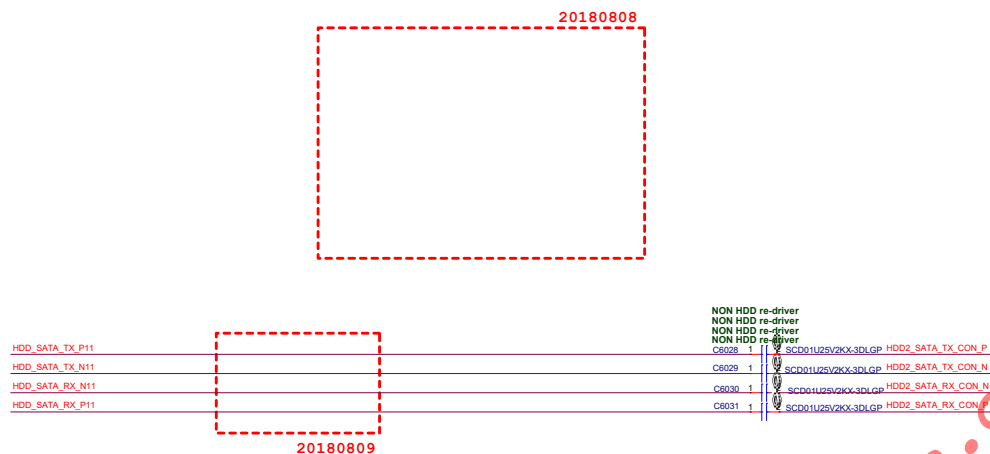
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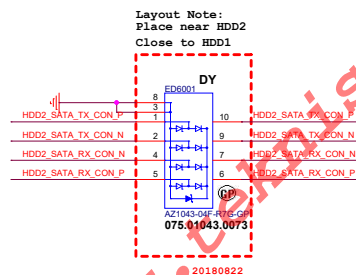
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
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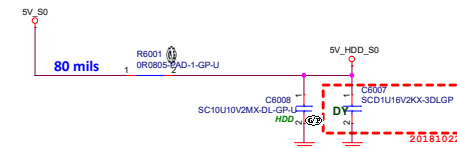
# SATA RE-DRIVER



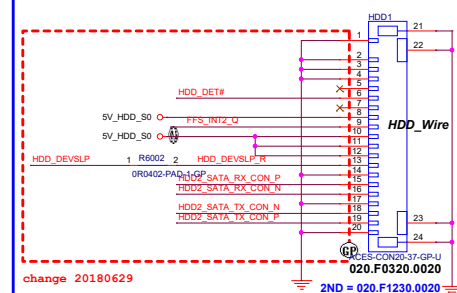
## HDD ESD



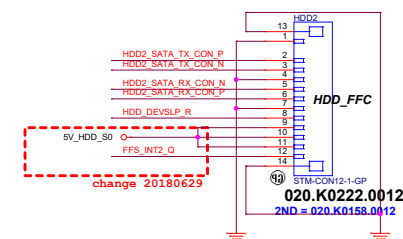
## HDD POWER



## SATA HDD Connector

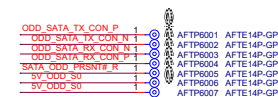
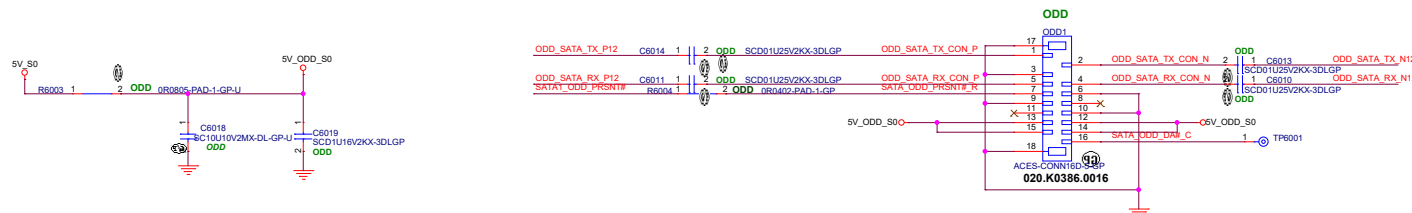


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	



**Main Func = ODD**

ODD



**BOLT L 14 EMMC**



Title	<b>SATA IDE HDD/ODD</b>
-------	-------------------------

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**Main Func = WLAN**

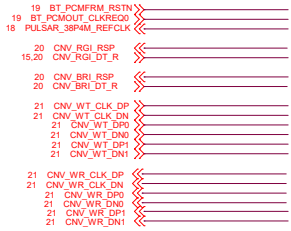
## BT



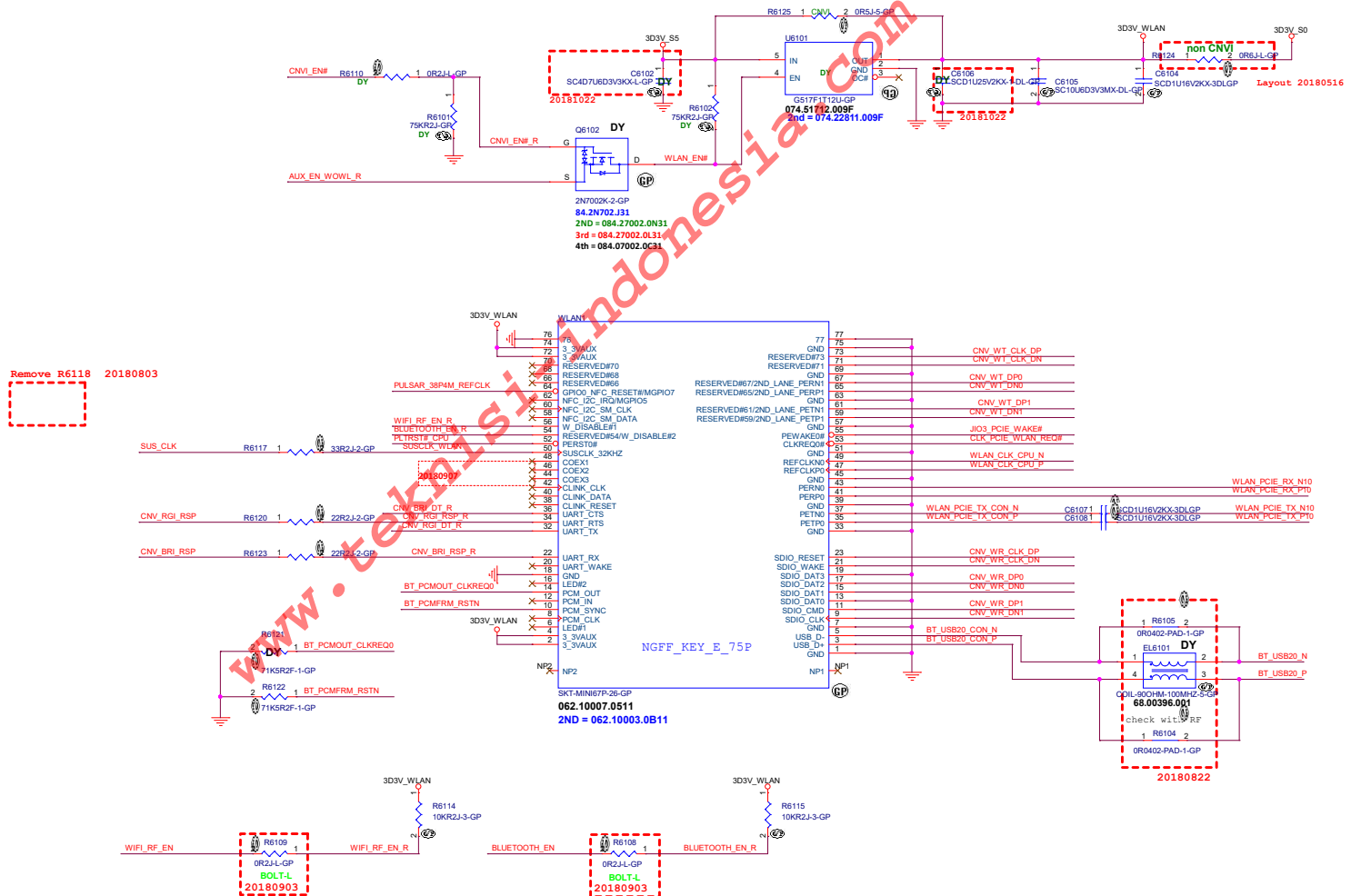
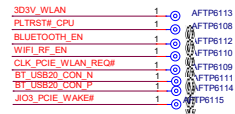
## WLAN



CNVI



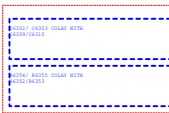
## Others



CPU		WLAN
GPP_F8_RXD	COEX1	UART TXD
GPP_F9_TXD	COEX2	UART RXD
GPP_F0_BLANKING	COEX3	STANDARD PIN

# 1





2018080-

**ESD** FOR ESD\_R2 SKU, 千萬計得BOM要手動!

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

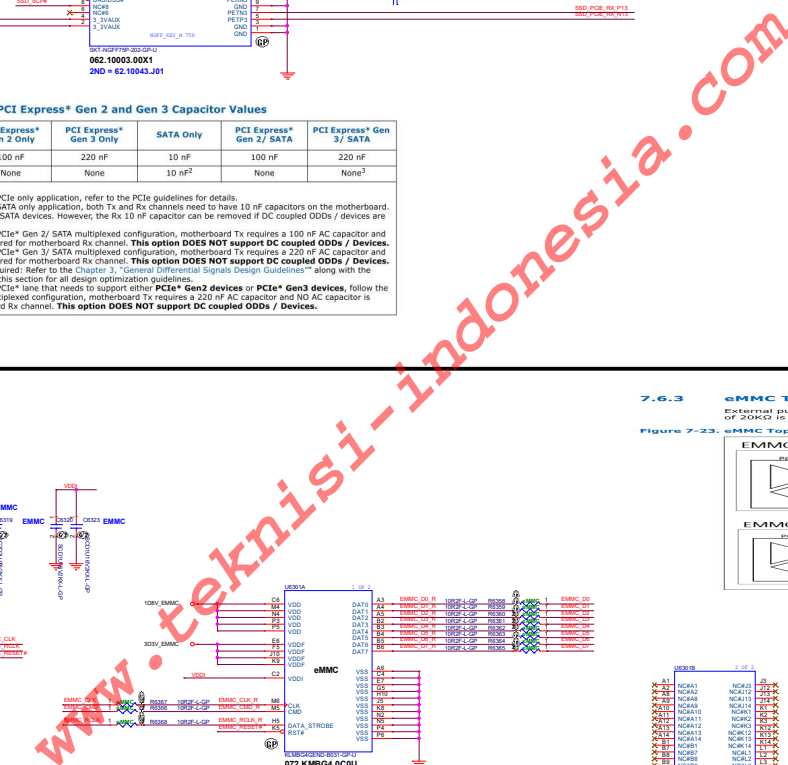
74	Yes	Yes	Yes
75	Yes	Yes	Yes
76	Yes	Yes	Yes
77	Yes	Yes	Yes
78	Yes	Yes	Yes
79	Yes	Yes	Yes
80	Yes	Yes	Yes
81	Yes	Yes	Yes
82	Yes	Yes	Yes
83	Yes	Yes	Yes
84	Yes	Yes	Yes
85	Yes	Yes	Yes
86	Yes	Yes	Yes
87	Yes	Yes	Yes
88	Yes	Yes	Yes
89	Yes	Yes	Yes
90	Yes	Yes	Yes
91	Yes	Yes	Yes
92	Yes	Yes	Yes
93	Yes	Yes	Yes
94	Yes	Yes	Yes
95	Yes	Yes	Yes
96	Yes	Yes	Yes
97	Yes	Yes	Yes
98	Yes	Yes	Yes
99	Yes	Yes	Yes
100	Yes	Yes	Yes
101	Yes	Yes	Yes
102	Yes	Yes	Yes
103	Yes	Yes	Yes
104	Yes	Yes	Yes
105	Yes	Yes	Yes
106	Yes	Yes	Yes
107	Yes	Yes	Yes
108	Yes	Yes	Yes
109	Yes	Yes	Yes
110	Yes	Yes	Yes
111	Yes	Yes	Yes
112	Yes	Yes	Yes
113	Yes	Yes	Yes
114	Yes	Yes	Yes
115	Yes	Yes	Yes
116	Yes	Yes	Yes
117	Yes	Yes	Yes
118	Yes	Yes	Yes
119	Yes	Yes	Yes
120	Yes	Yes	Yes
121	Yes	Yes	Yes
122	Yes	Yes	Yes
123	Yes	Yes	Yes
124	Yes	Yes	Yes
125	Yes	Yes	Yes
126	Yes	Yes	Yes
127	Yes	Yes	Yes
128	Yes	Yes	Yes
129	Yes	Yes	Yes
130	Yes	Yes	Yes
131	Yes	Yes	Yes
132	Yes	Yes	Yes
133	Yes	Yes	Yes
134	Yes	Yes	Yes
135	Yes	Yes	Yes
136	Yes	Yes	Yes
137	Yes	Yes	Yes
138	Yes	Yes	Yes
139	Yes	Yes	Yes
140	Yes	Yes	Yes
141	Yes	Yes	Yes
142	Yes	Yes	Yes
143	Yes	Yes	Yes
144	Yes	Yes	Yes
145	Yes	Yes	Yes
146	Yes	Yes	Yes
147	Yes	Yes	Yes
148	Yes	Yes	Yes
149	Yes	Yes	Yes
150	Yes	Yes	Yes
151	Yes	Yes	Yes
152	Yes	Yes	Yes
153	Yes	Yes	Yes
154	Yes	Yes	Yes
155	Yes	Yes	Yes
156	Yes	Yes	Yes
157	Yes	Yes	Yes
158	Yes	Yes	Yes
159	Yes	Yes	Yes
160	Yes	Yes	Yes
161	Yes	Yes	Yes
162	Yes	Yes	Yes
163	Yes	Yes	Yes
164	Yes	Yes	Yes
165	Yes	Yes	Yes
166	Yes	Yes	Yes
167	Yes	Yes	Yes
168	Yes	Yes	Yes
169	Yes	Yes	Yes
170	Yes	Yes	Yes
171	Yes	Yes	Yes
172	Yes	Yes	Yes
173	Yes	Yes	Yes
174	Yes	Yes	Yes
175	Yes	Yes	Yes
176	Yes	Yes	Yes
177	Yes	Yes	Yes
178	Yes	Yes	Yes
179	Yes	Yes	Yes
180	Yes	Yes	Yes
181	Yes	Yes	Yes
182	Yes	Yes	Yes
183	Yes	Yes	Yes
184	Yes	Yes	Yes

**Table 13-11. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values**

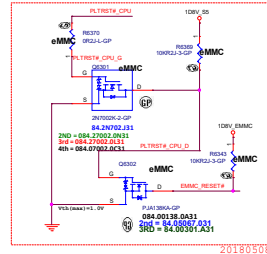
Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled D0s / Devices are not used.
3. Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 10 nF AC capacitor and motherboard requires a resistor for Rx channel. Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the Design Constraints.
4. Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 22 nF AC capacitor and motherboard requires a resistor for Rx channel. Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the Design Constraints.
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the Design Constraints.
6. Design Constraint: For PCIe\* lane that needs to support either **PCIe\* Gen2 devices or PCIe\* Gen3 devices**, follow the PCIe\* Gen 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784,



Layout note: R6370 close to CPU



20180503

### 6.2.1 Power supply: eMMC\*

In the eMMC\*,  $V_{CC}$  is used for the NAND flash device and its interface voltage;  $V_{CCQ}$  is for the controller and the MMC interface voltage shown in Figure 9. The core regulator is optional and only required when internal core logic voltage is regulated from  $V_{CCQ}$ . A  $C_{dec}$  capacitor must be connected to the  $V_{out}$  terminal to stabilize regulator output on the system.

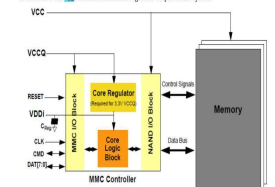
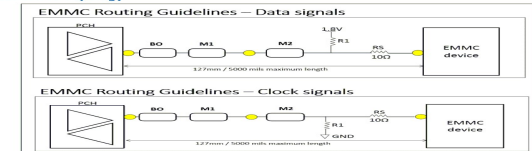


Figure 9 - eMMC™ Internal Power Diagram

### 7.6.3 eMMC Topology Guidelines

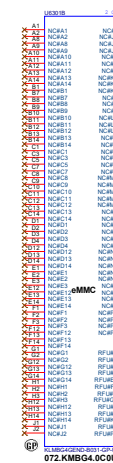
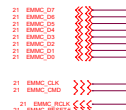
External pull-up resistors of 20K $\Omega$  are required on the Data lines. A pull-down resistor of 20K $\Omega$  is recommended on the Clock and RCLK lines.

**Figure 7-23. eMMC Topology**



20180809

Main Func = eMMC



**GP** KLMBG4GEND-8031-GP-  
072.KMBG4.0C01

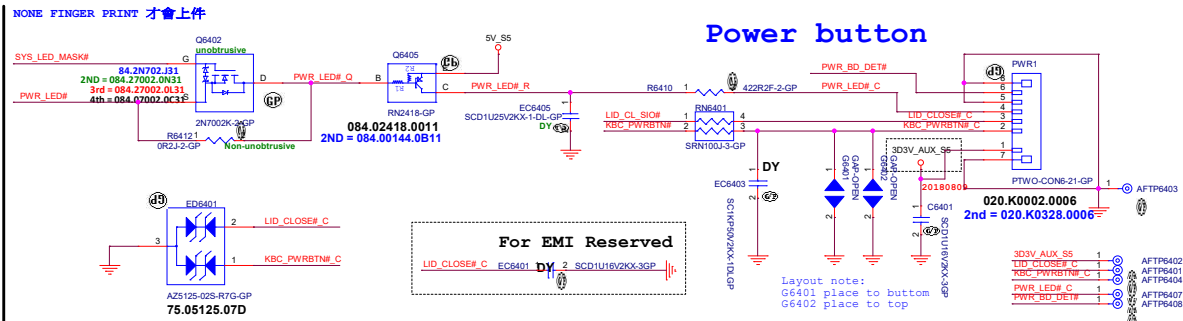
BOLT L 14 EMK



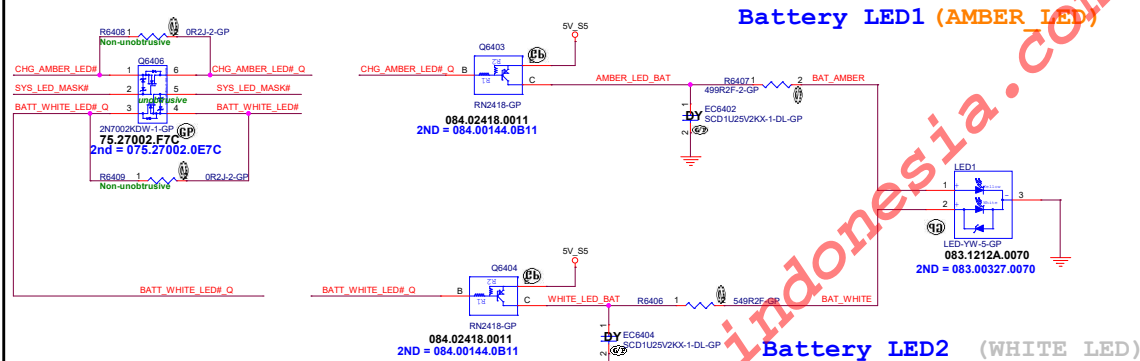
```

24 PWR_LED# >>>_____
20,21 PWR_BD_DET# <<<_____
24,92 LID_CL_SIO# <<<_____
24,92 KBC_PWRBTN# <<<_____

```



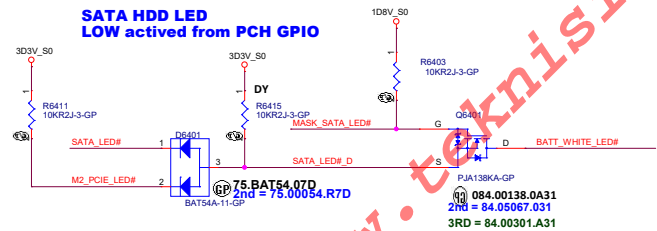
Low activated from KBC GPIO



```

24 MASK_SATA_LED# >>>_____
    16 SATA_LED# >>>_____
    63 M2_PCIE_LED# <<<_____

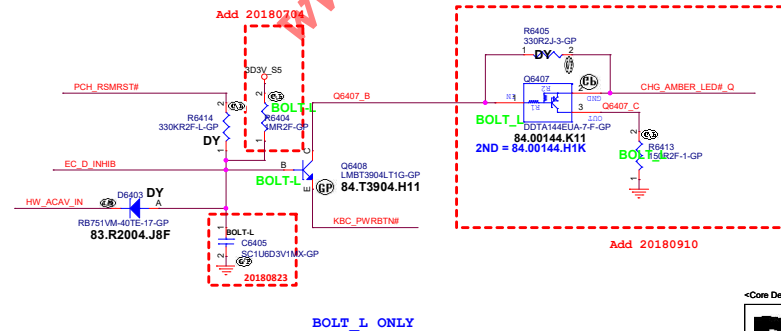
```



```

17,24 PCH_RSMRST# >>> _____
      EC_D_INHIB  >>> _____
24,43,44 HW_ACAV_IN >>> _____

```



24 CAP\_LED#\_R >>>

24 KSI[0..7] >>>

24 KSO[0..16] <<<

20 KB\_DET# <<<

9 KB\_LED\_BI\_DET <<<

24 KB\_LED\_PWM >>>

[illegible]

LOW active from KBC GPIO

5V\_50

CAP\_LED\_R

Q105 BC107

CAP\_LED\_G

R1 1K

R2 1K

084.02418.0011

2ND = 084.00144.0B11

BY C506 SC10F50V2JN-4DLGP

Diagram of the ACES CON30-29-GP connector showing pin assignments for AFTR541 through AFTR657. The connector is a 30-pin D-sub connector. Pins 1-15 are on the left, and pins 16-30 are on the right. A legend indicates: 1 = CAP LED, 2 = X, 3 = X. The pin assignments are:

Pin	Assignment
1	K5010
2	K5011
3	K5012
4	K5013
5	K5014
6	K5015
7	K5016
8	K5017
9	K5018
10	K5019
11	K5020
12	K5021
13	K5022
14	K5023
15	K5024
16	K5025
17	K5026
18	K5027
19	K5028
20	K5029
21	K5030
22	K5031
23	K5032
24	K5033
25	K5034
26	K5035

Legend: 1 = CAP LED, 2 = X, 3 = X.

ACES CON30-29-GP  
**020.K0254.0030**  
**2nd = 020.K0274.0030**  
**3rd = 20.K0750.030**

24 TP\_EN# >>> \_\_\_\_\_

24 CLK\_TP\_SIO <<< \_\_\_\_\_  
24 DAT\_TP\_SIO <<< \_\_\_\_\_

I2C0\_SCL\_TCH\_PAD <<< \_\_\_\_\_  
I2C0\_SDA\_TCH\_PAD <<< \_\_\_\_\_

24 TP\_WAKE\_KBC# <<< \_\_\_\_\_  
24 PTP\_DIS# >>> \_\_\_\_\_

TP side has pull high

TP\_WAKE KBC# 1 R6511 2 TP\_WKA

10KR2J-3-GF

**Precision Touch Pad Connector**

TP\_VDD

C5505

I2C1\_VDD

I2C1\_SDA\_R

I2C1\_SCL\_R

TP\_WAKE\_RSCW#

PTP\_DIS#

TPDATA\_C

TPCLK\_C

APTPE51

TP1

10

9

8

7

6

5

4

3

2

1

0

ACES-CONB-66-CP

020.K0151.0008

2ND = 020.K0255.0008

TP\_VDD

TPCLK\_C

TPDATA\_C

I2C1\_SCL\_R

I2C1\_SDA\_R

TP\_WAKE\_RSCW#

PTP\_DIS#

APTPE52

APTPE56

APTPE59

APTPE60

APTPE624

APTPE628

APTPE627

APTPE625

APTPE58

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



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Size  
A4

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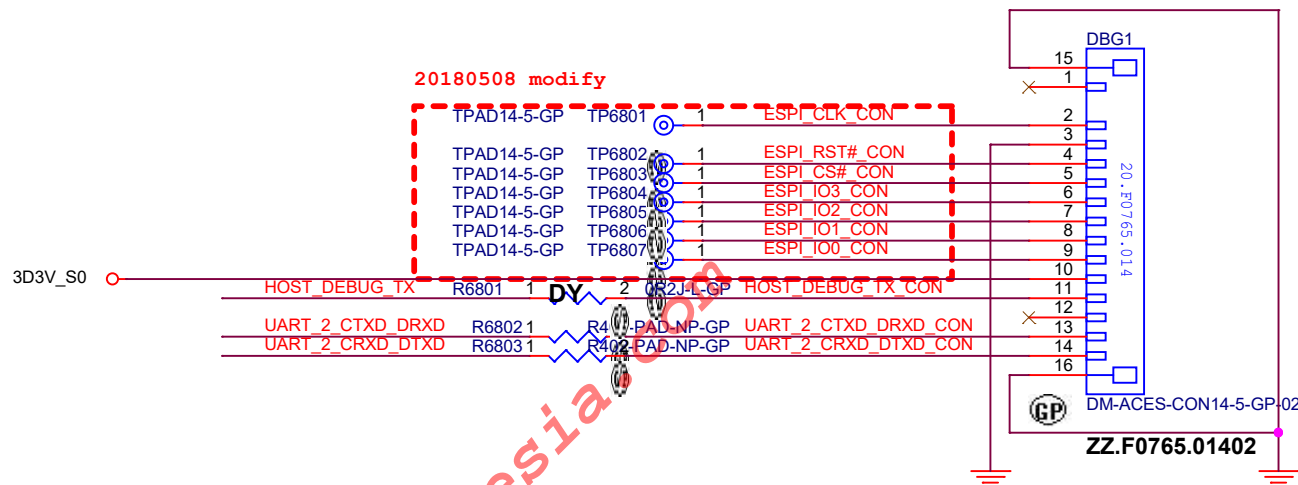
Rev  
**1**

Date: Thursday, December 27, 2018

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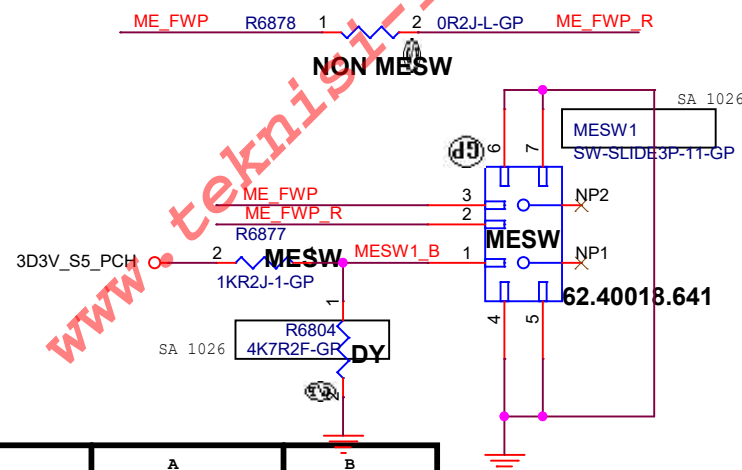
# Main Func = Debug

## Debug Connector



24 HOST\_DEBUG\_TX >>>  
20 UART\_2\_CTXD\_DRXD >>>  
20 UART\_2\_CRXD\_DTXD <<<

## Firmware SW



24 ME\_FWP <<<  
19 ME\_FWP\_R <<<

MESW1\_B 1 AFTP6801 AFTE14P-GP  
ME\_FWP\_R 1 AFTP6802 AFTE14P-GP  
ME\_FWP 1 AFTP6803 AFTE14P-GP

	A	B
ME_FWP_R	Low	High
	Normal Operation (Default)	Override

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12,13,18,56	PCH_SMBDATA	<< >> —————
12,13,18,56	PCH_SMBCLK	<< >> —————

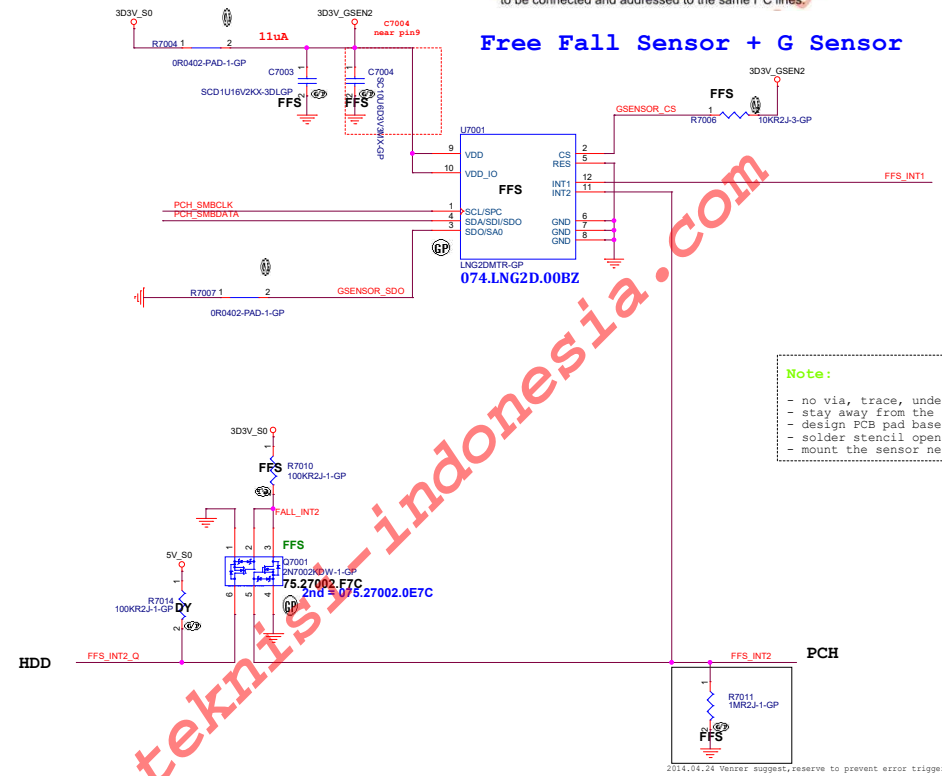
```

18  FFS_INT1  <<<————
20  FFS_INT2  <<<————

60  FFS_INT2_Q <<<————

```

### Free Fall Sensor + G Sensor



- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design FCB pad based on our sensor LGA pad size (add 0.1mm)
- mount stencil opening to 90% of the FCB pad size
- solder the sensor near the center of mass of the NB as possible as you can

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

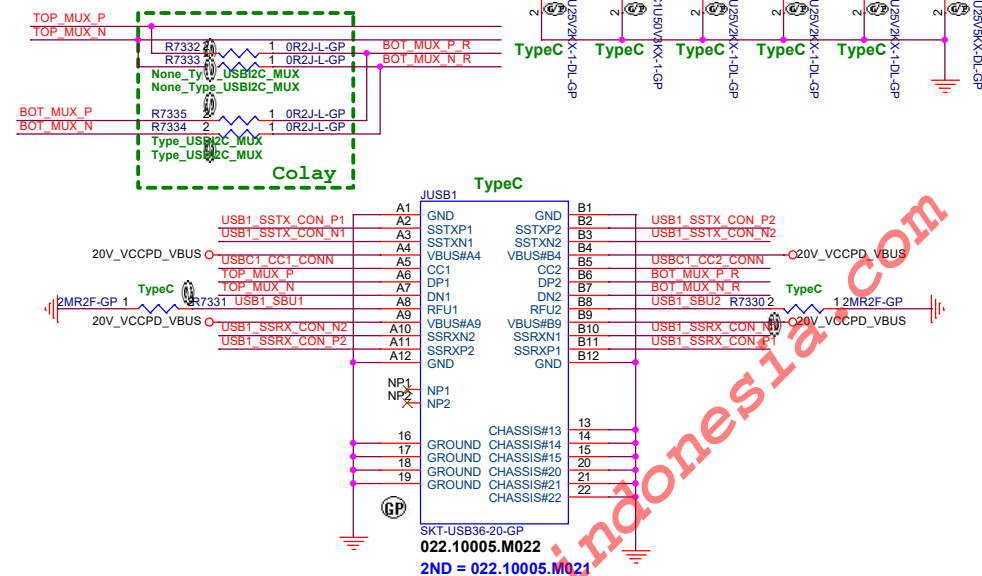






# Main Func = TYPEC CONNECTOR

## Type-C Connector

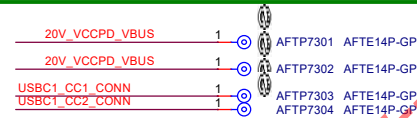


71 USB1\_SSRX\_CON\_N1 <<<<  
 71 USB1\_SSRX\_CON\_P1 <<<<  
 71 USB1\_SSRX\_CON\_N2 <<<<  
 71 USB1\_SSRX\_CON\_P2 <<<<  
 71 USB1\_SSTX\_CON\_N1 >>>>  
 71 USB1\_SSTX\_CON\_P1 >>>>  
 71 USB1\_SSTX\_CON\_N2 >>>>  
 71 USB1\_SSTX\_CON\_P2 >>>>

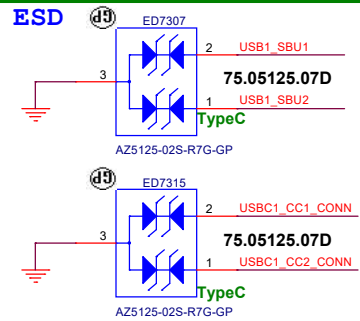
71 USB1\_SBU1 >>>>  
 71 USB1\_SBU2 >>>>  
 72 USBC1\_CC1\_CONN >>>>  
 72 USBC1\_CC2\_CONN >>>>

### From USB2.0/ I2C Mux

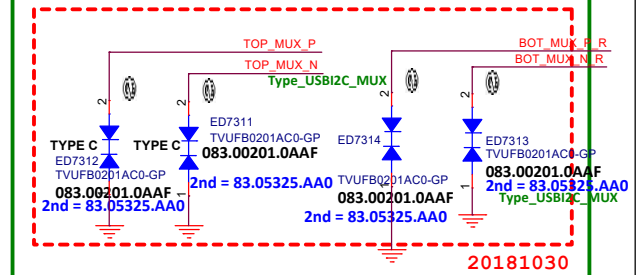
71 TOP\_MUX\_P <<>>  
 71 TOP\_MUX\_N <<>>  
 71 BOT\_MUX\_P <<>>  
 71 BOT\_MUX\_N <<>>



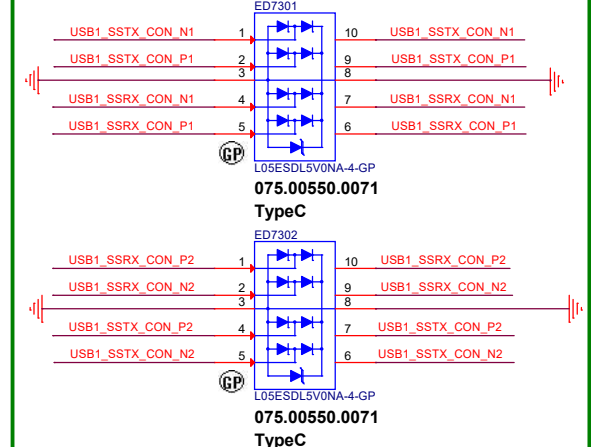
## CC & SBU ESD



## USB2.0 ESD



## USB3.1 ESD



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Title		
TYPEC CONN		
Size	Document Number	Rev
A3	BOLT WHL	1
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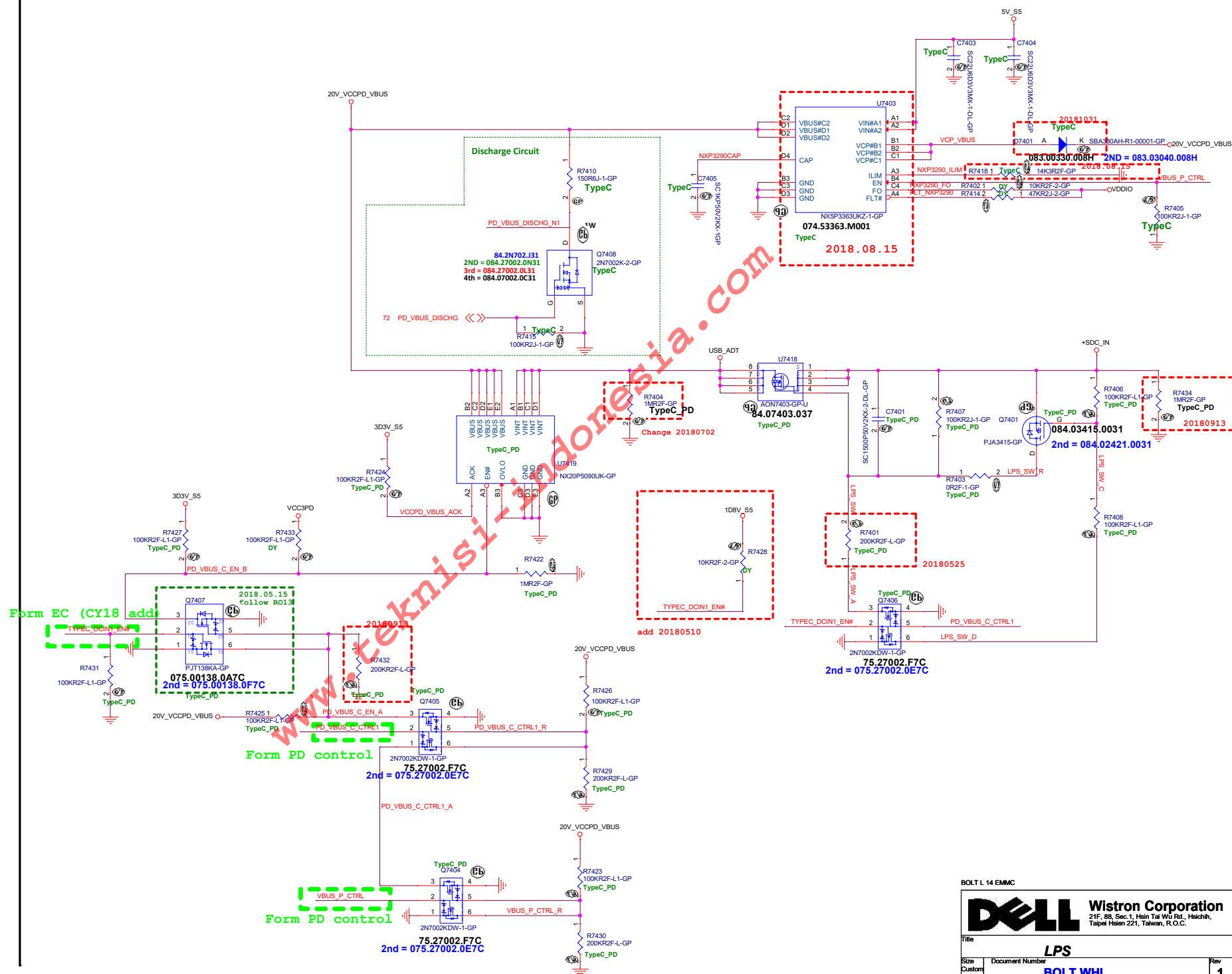
**Main Func = LPS**

```

72 PD_VBUS_C_CTRL1 >>>_____
72 VBUS_P_CTRL >>>_____
24 TYPEC_DCIN1_EN# >>>_____
72 NXP3290_FO <<<_____

```

44 VCCPD VBUS ACK &gt;&gt;\_\_\_\_\_




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GPU(2/5)DIGITALOUT			
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Part			
GPU(3/5)VRAM/F			
Rev	Document Number		
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Title		GPU-VRAM1,2 (1/4)	
Size	Document Number	Rev	
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Title		<b>GPU-VRAM3.4 (2/4)</b>	
Size A2	Document Number <b>BOLT WHL</b>	Rev <b>1</b>	
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**GPU-VRAM5,6 (3/4)**

Size	A3
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Document Number	
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1

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GPU-VRAM7,8 (4/4)

Size

A3

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**VGA Power B**

BOLT L 14 ENBA

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Part		
DISCRETE VGA POWER		
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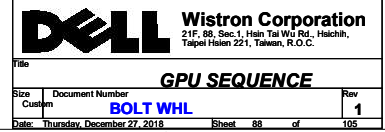


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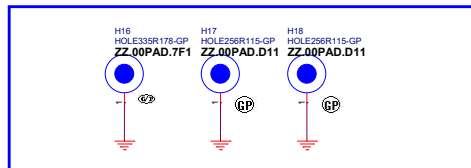
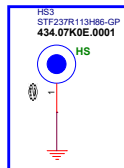
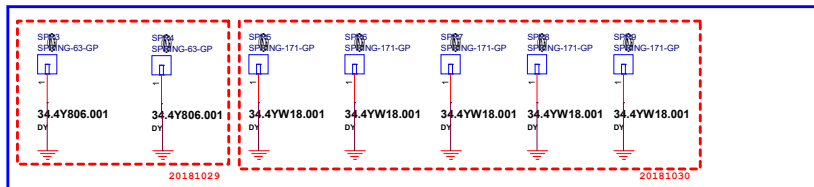
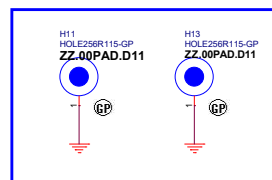
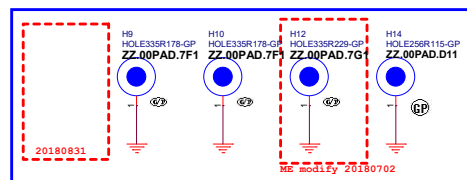
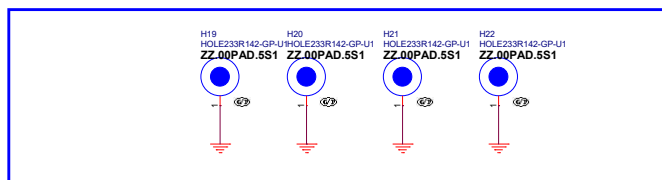
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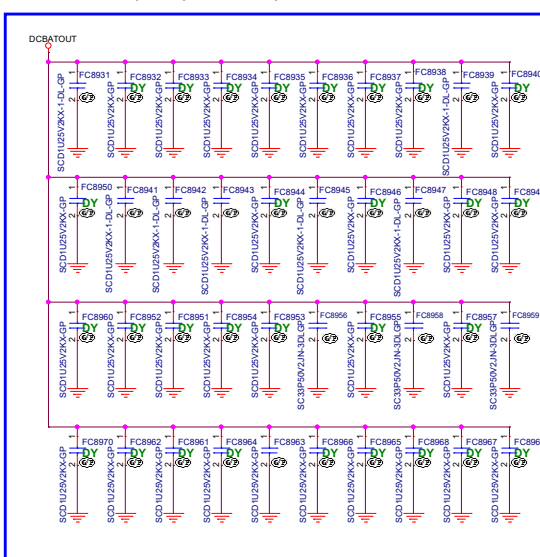
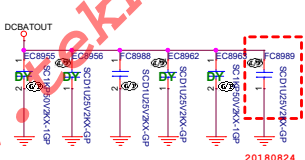
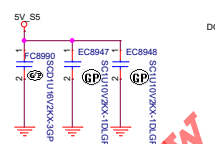
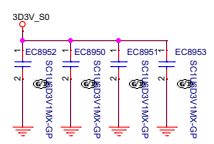
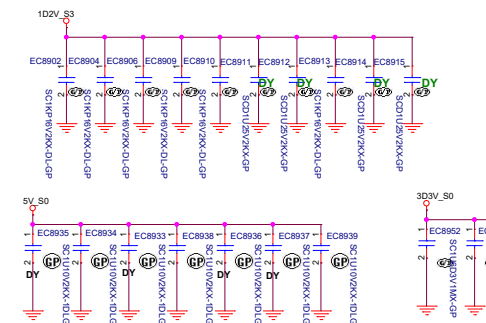
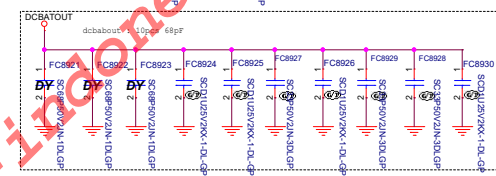
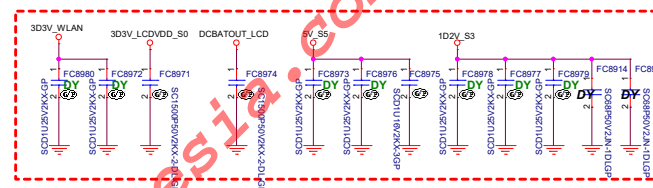
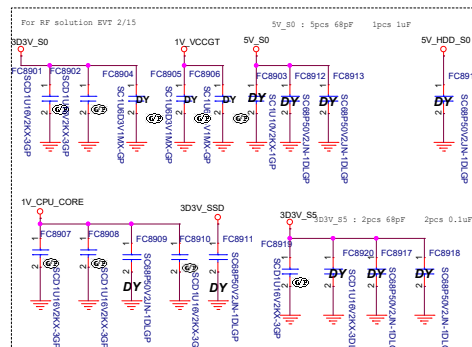
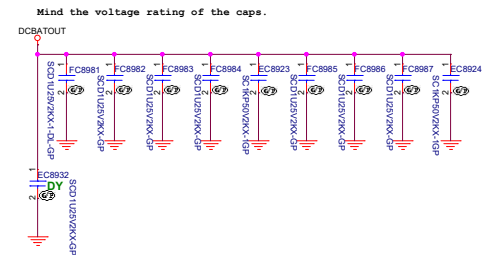
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# Main Func = UnusedParts



# Main Func = EMI & RF Capacitors



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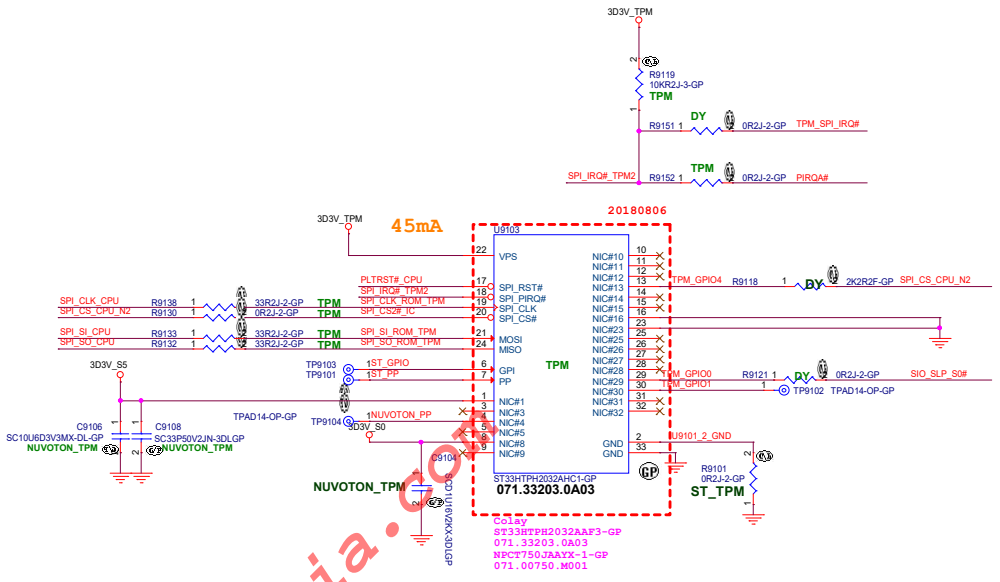
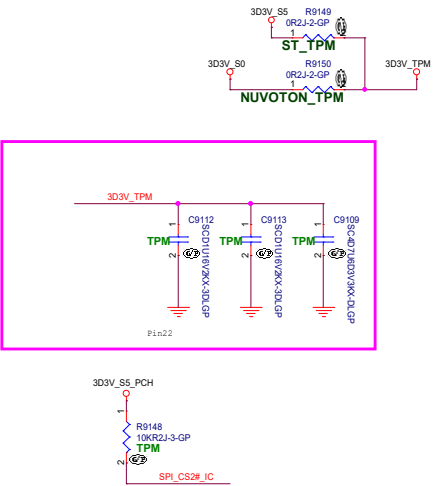


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Main Func = TPM

- 18,25 SPI\_SO\_CPU <<<
- 18,25 SPI\_CLK\_CPU >>>
- 15,18,25 SPI\_SI\_CPU >>>
- 18 SPI\_CS\_CPU\_N2 <<<
- 17,26,31,61,62,63 PLTRST#\_CPU >>>
- 17,40 SIO\_SLP\_S0# >>>
- 20 PIRQ# <<<
- 18 TPM\_SPI\_IRQ# <<<



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	DY	DY

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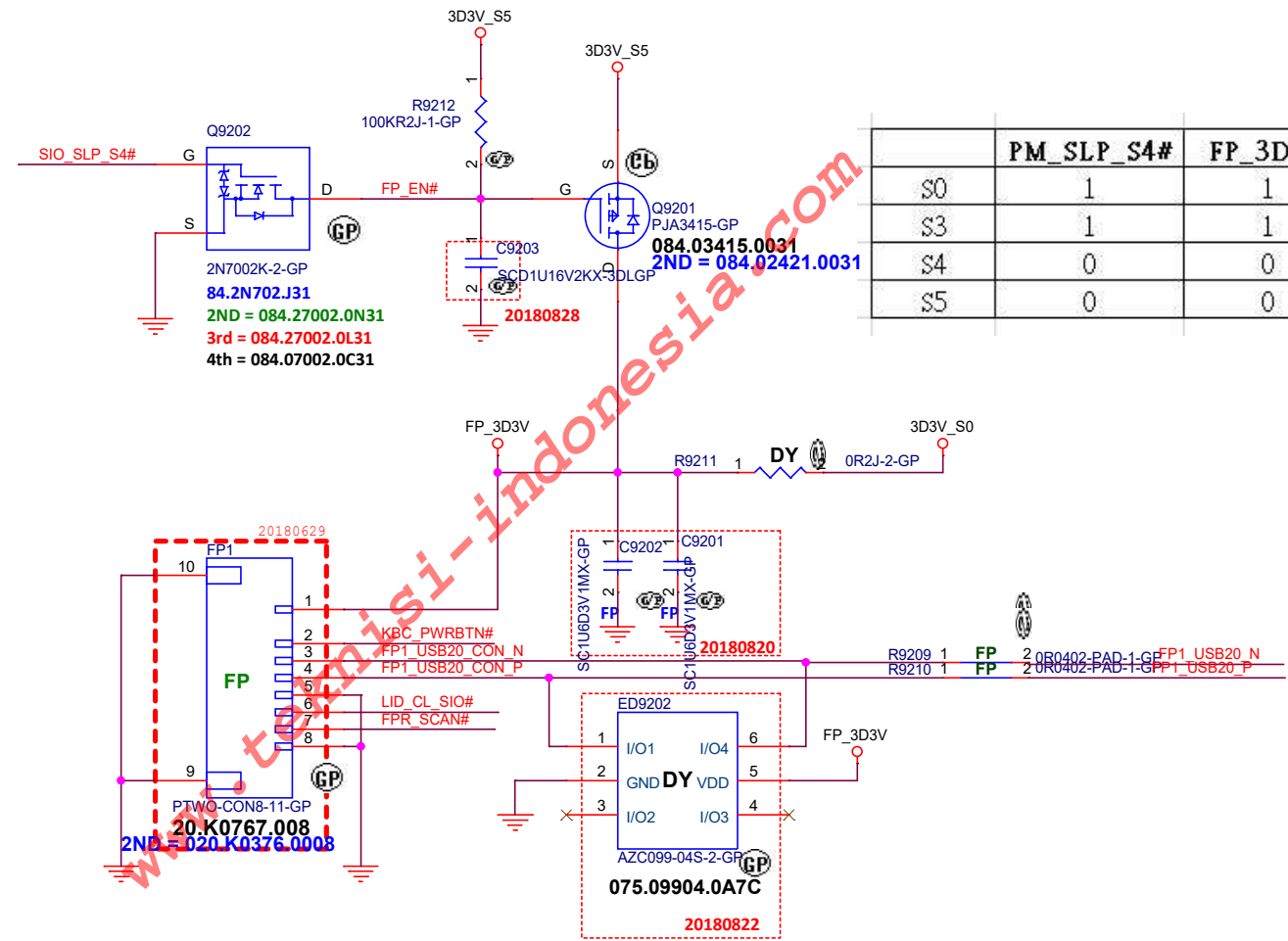
File **TPM2.0**

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Main Func = Finger Print


FBR(Botton side finger Print Sensor)

16 FP1\_USB20\_N >>>  
16 FP1\_USB20\_P >>>  
17,40,51 SIO\_SLP\_S4# >>>  
24,64 KBC\_PWRBTN# >>>  
24 FPR\_SCAN# >>>  
24,64 LID\_CL\_SIO# <<<



	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

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Title

**(Reserved)Finger Print**

Size

Document Number

Custom

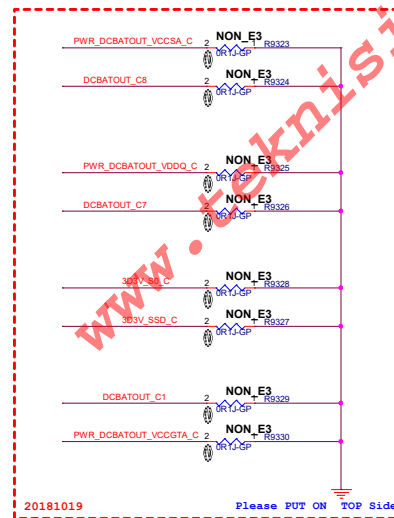
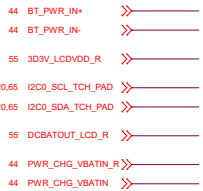
**BOLT WHL**

Date: Thursday, December 27, 2018

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Rev  
**1**

CH4 LCDBAT  
CH3 LCDVDD  
CH6 VCORE  
CH5 BATTERY



	WHL
P1+/-	CPU_VCCGT (iGPU Core) <input>
P2+/-	STORAGE (SSD/HDD) <output>
P3+/-	DISPLAY_CTLR <output>
P4+/-	DISPLAY_BACKLIGHT <output>
P5+/-	SYSTEM (battery leads)
P6+/-	CPU_VCORE <input>
P7+/-	CPU_VDDQ (MCU Core) <input>
P8+/-	CPU_VCCSA (PCH Core) <input>

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19





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LVDS_Switch			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>1</b>
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Main Func = Firmware SW

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Title

**Firmware SW**

Size  
A4

Document Number  
**BOLT WHL**

Rev  
**1**

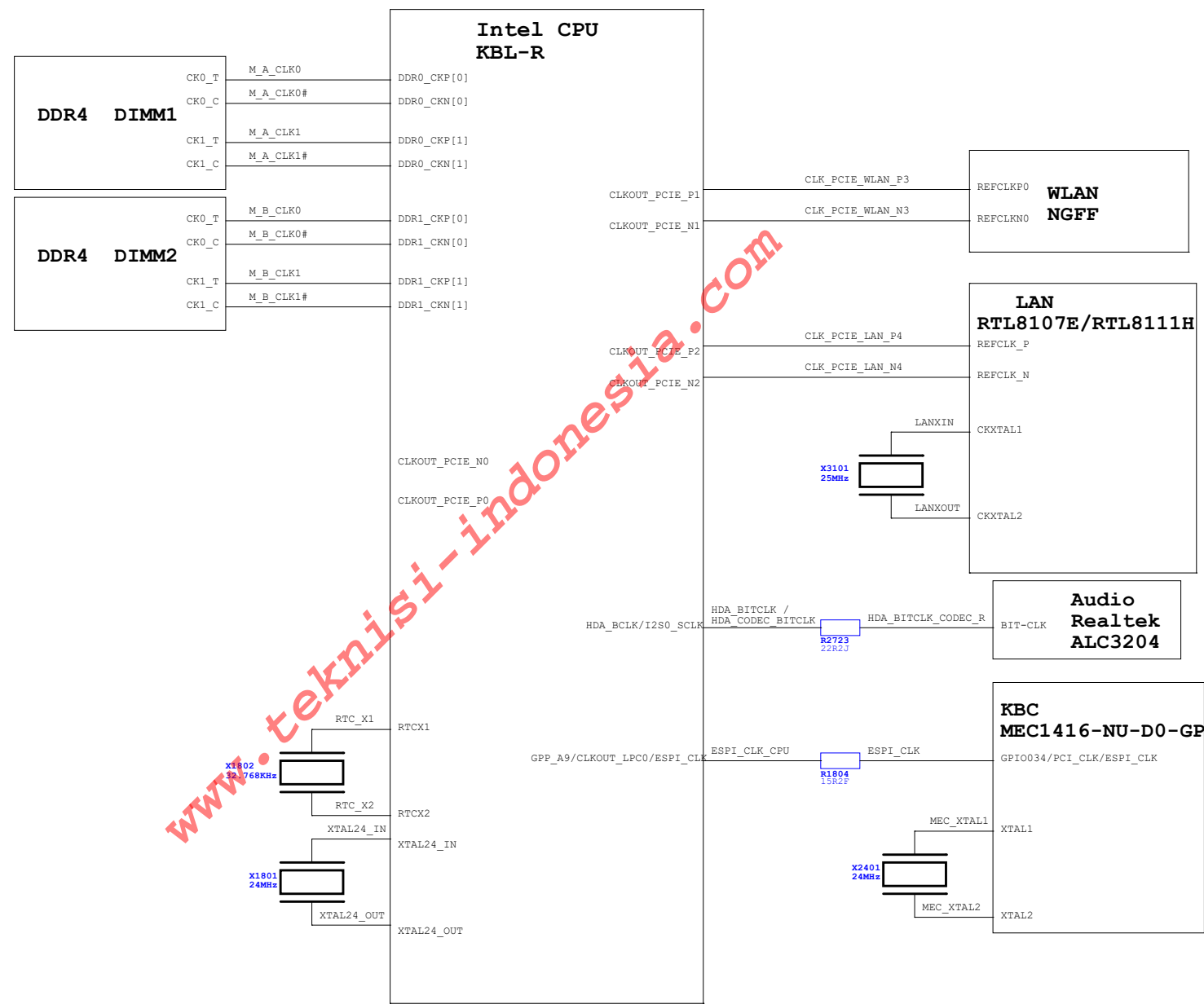
Date: Thursday, December 27, 2018

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CLK Block Diagram



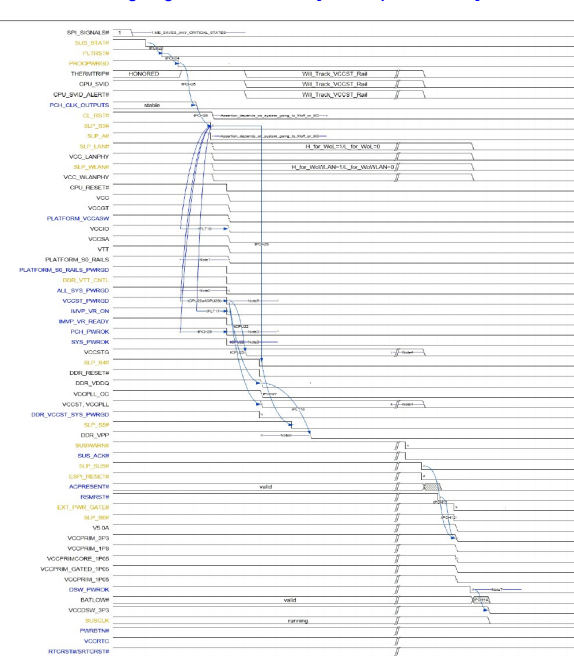
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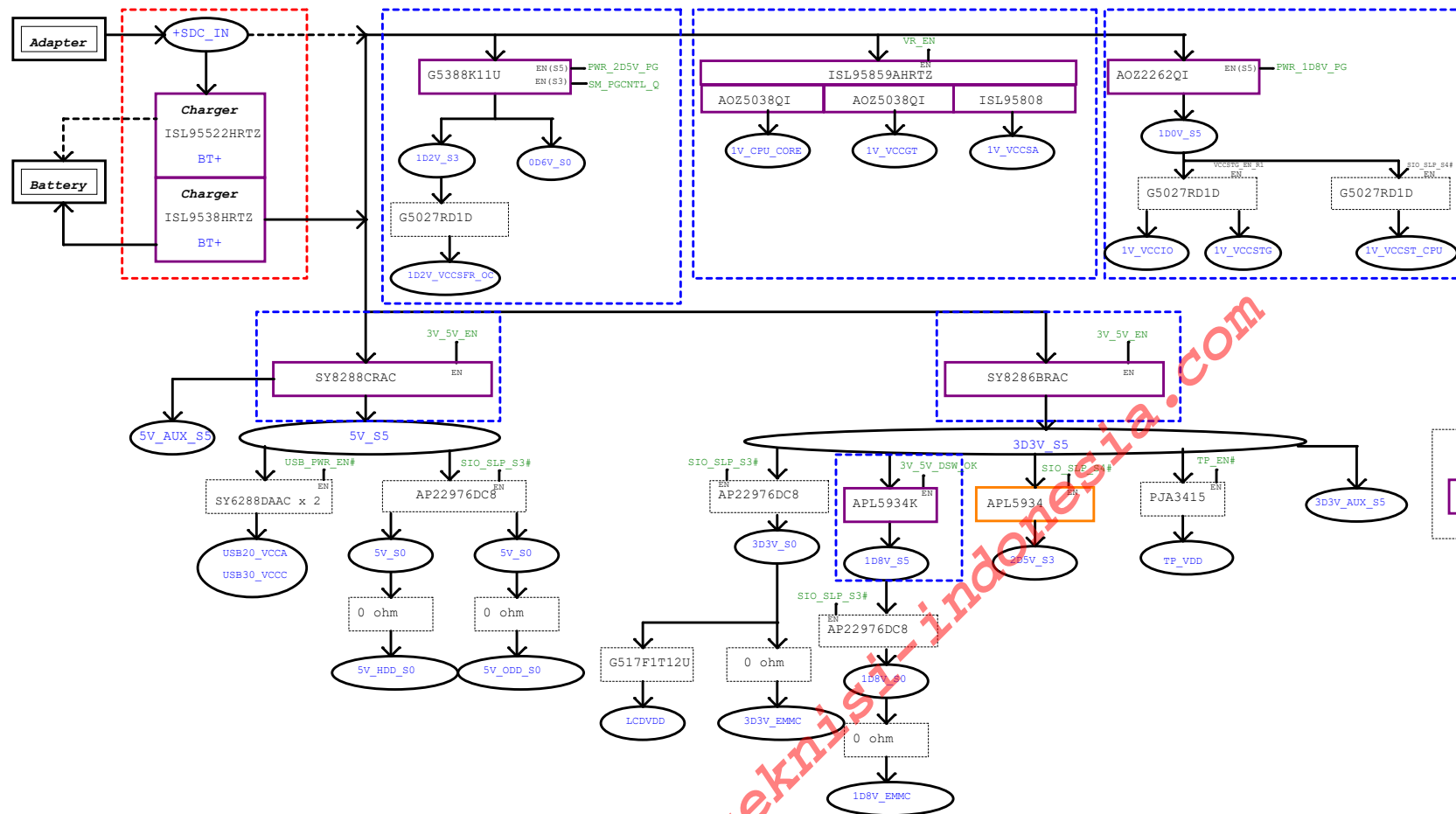
**BOLT WHL**

Sheet	101	of	105
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WHL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]





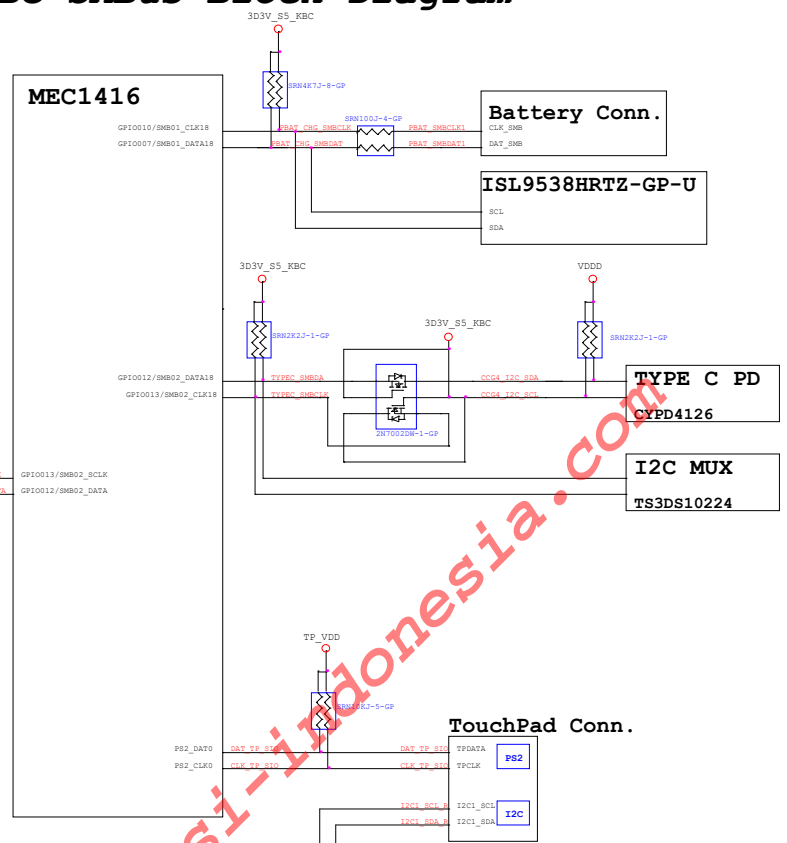
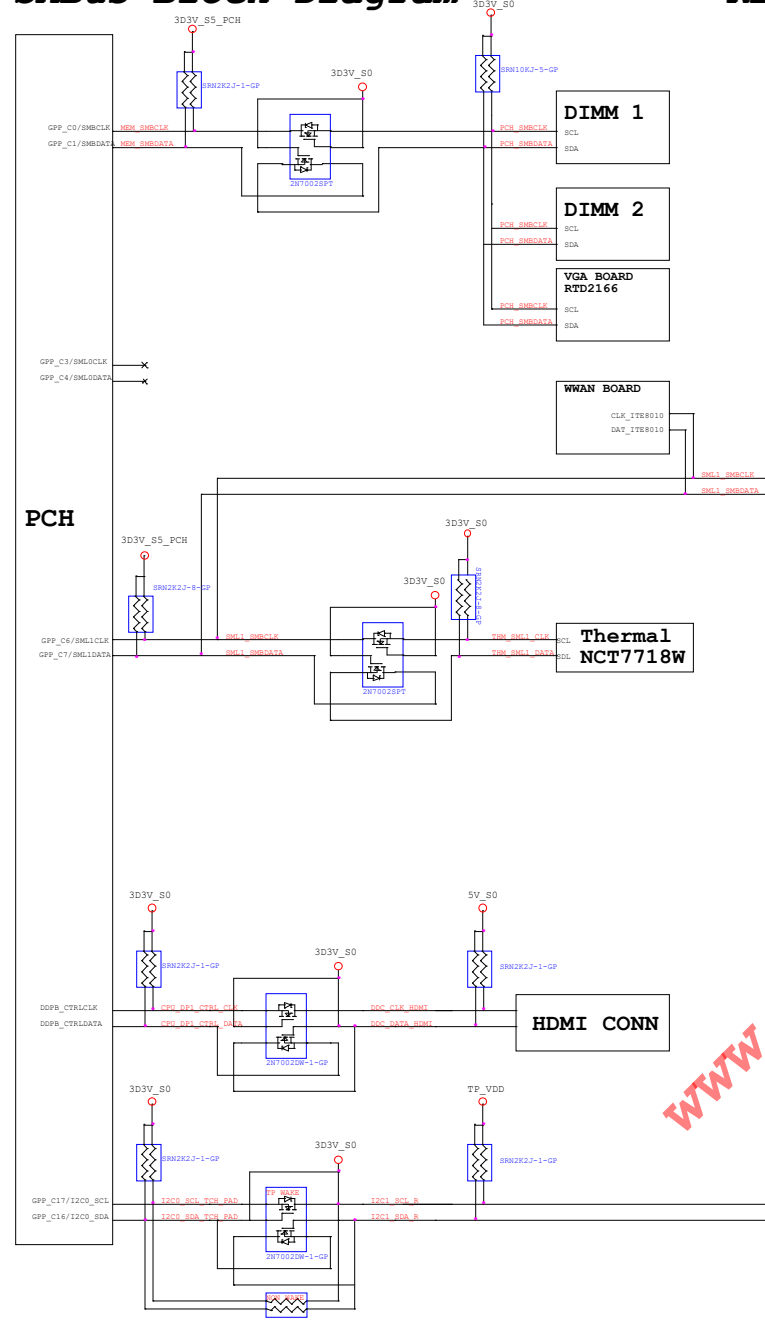


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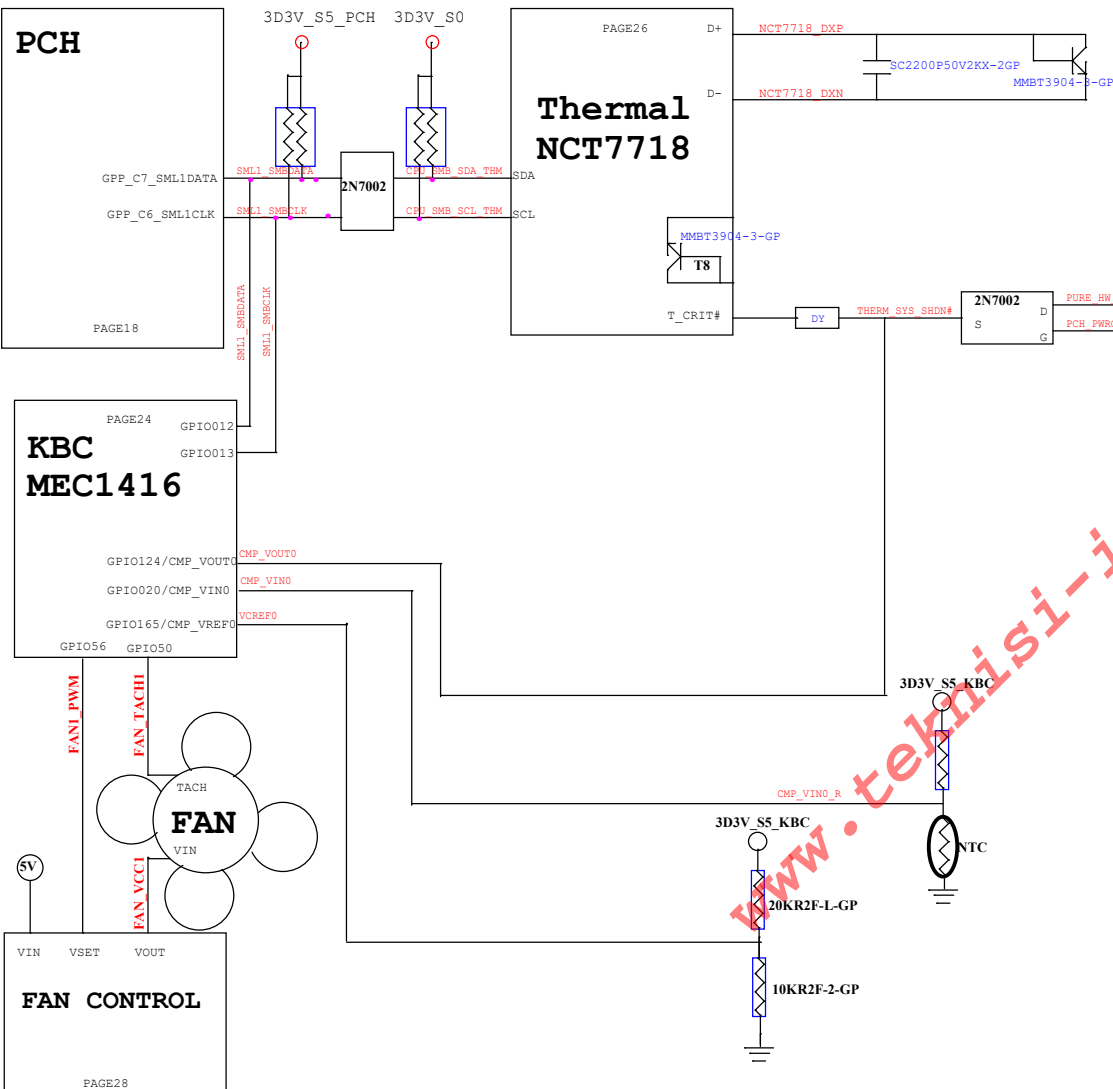
# PCH SMBus Block Diagram

# KBC SMBus Block Diagram



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# Thermal Block Diagram



# Audio Block Diagram

